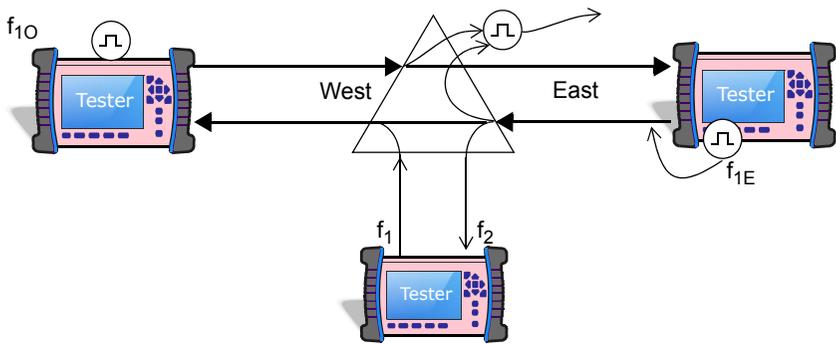


Network Synchronization (jitter & wander explained)

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Contents

Chapter 1 Classic SDH/SONET	1
1.1 The Emergence of SDH/SONET Networks	1
1.1.1 Limitations of Plesiochronous Networks	1
1.1.2 The SDH/SONET Challenge	3
1.2 Comparison of SDH and SONET	5
1.3 Functional Architecture	6
1.3.1 Network Elements	6
1.3.2 Network Topology	7
1.3.3 Topology Partitioning	8
1.3.4 SDH/SONET Layers	8
1.4 SDH/SONET Formats and Procedures	11
1.4.1 SDH/SONET Frame Structure	12
1.4.2 Multiplexing Map	15
1.5 SDH Transport Services	15
1.6 Transporting PDH/T-Carrier Tributaries	19
1.6.1 Transport on VC-4 or STS-3c SPE	20
1.6.2 Transport on VC-3	21
1.6.3 Transport of 2-Mbit/s Circuits	23
1.7 Pointers and Timing Compensation	26
1.7.1 Payload Synchronization	26
1.7.2 Pointer Formats and Procedures	27
1.8 Overheads	30
1.8.1 Path Overhead	32
1.8.2 Section Overhead	33
1.8.3 The SDH/SONET Hierarchy	35
1.9 Concatenation	37
1.10 Maintenance	38
1.10.1 SDH/SONET Events	38
1.10.2 Monitoring Events	41
1.10.3 Event Tables	41
1.11 Performance Monitoring	44
1.11.1 Bit Error Checking	44

1.11.2	Tandem Connection Monitoring	45
1.11.3	Forward Error Correction	45
1.12	Defects	46
1.13	SDH Resilience	49
1.13.1	Protection Basics	50
1.13.2	Multiplex Section or Line Protection	53
1.14	Operation, Administration, and Management	57
1.14.1	The TMN Standard	57
1.14.2	TMN Benefits	58
Chapter 2 Network Synchronization.....		61
2.1	Architecture of Synchronization Networks.....	61
2.1.1	Synchronization Network Topologies	63
2.2	Interconnection of Nodes	65
2.2.1	Synchronization Signals	65
2.2.2	Holdover Mode	67
2.2.3	Global Positioning System	67
2.3	Disturbances in Synchronization Signals.....	68
2.3.1	Frequency Offset	68
2.3.2	Phase Fluctuation	70
2.4	Synchronization of Transmission Networks	73
2.4.1	Synchronization in SONET and SDH	74
2.4.2	Synchronization Models	75
2.4.3	Timing Loops	77
2.5	Digital Synchronization and Switching	77
2.6	SSU in a Synchronization Network	79
2.6.1	Functions of SSU	80
Chapter 3 Jitter and Wander Control.....		83
3.1	Dealing with Jitter.....	83
3.1.1	Phase Fluctuation	83
3.1.2	Jitter Metrics and Measurement	84
3.1.3	Measuring Jitter in Output Interfaces	87
3.1.4	Measuring Jitter Tolerance	88
3.1.5	Measuring Jitter Transfer	90
3.1.6	Mapping Jitter and Combined Jitter	93
3.1.7	Jitter in Leased Lines	96
3.2	Dealing with Wander.....	96
3.2.1	Synchronization of SDH/SONET Networks	97
3.2.2	Measuring Relative and Absolute Wander	97
3.2.3	The Metrics of Wander: TIE, MTIE, and TDEV	98
3.2.4	Measuring Output Wander	100
3.2.5	Measuring Tolerance to Input Wander	101
3.2.6	Measuring Wander Transfer	103
3.2.7	Response to Phase Transients	103

3.2.8	Operating in Holdover Mode	105
3.3	Tests on ADMs and Cross-connects.....	107
3.3.1	Measuring Jitter	107
3.3.2	Synchronization Tests	109

Chapter 1

Classic SDH/SONET

Synchronous digital hierarchy (SDH) is an ITU-T universal standard that defines a common and reliable architecture for transporting telecommunications services on a worldwide scale. *Synchronous optical network* (SONET) is today a subset of SDH, promoted by *American National Standards Institute* (ANSI) and used in the U.S., Canada, Taiwan, and Korea.

From now on we will use the acronym *SDH* to refer to the generic ITU-T standard that includes also SONET.

1.1 THE EMERGENCE OF SDH/SONET NETWORKS

During the 1980s, progress in optical technologies and microprocessors offered new challenges to telecommunications in terms of bandwidth and data processing. At that time, plesiochronous hierarchies (T-carrier and PDH) dominated transport systems, but a series of limitations and the necessity to introduce new transmission technologies moved to develop a new architecture.

Antitrust legislation was the final factor that hastened the development of SONET. It was applied to the telecommunications business and forced the giant, Bell, to be split up into small companies, the *regional Bell operating companies* (RBOCs). SONET, developed at Bellcore labs in 1984, grew out of the need to inter-connect RBOCs using standardized optical interfaces. Telecom liberalization was confirmed around the world during the '90s, and this has inevitably led to global competition and interoperation. In 1988, the *Comité Consultatif International Télégraphique Et Téléphonique* CCITT (now ITU) proposed creating *broadband-ISDN* (B-ISDN) to simultaneously transport data, voice, video, and multimedia over common transmission infrastructures. *Asynchronous transfer mode* (ATM) was selected for the switching layer, and SDH for transport at the physical layer.

1.1.1 Limitations of Plesiochronous Networks

Plesiochronous networks have the following limitations:

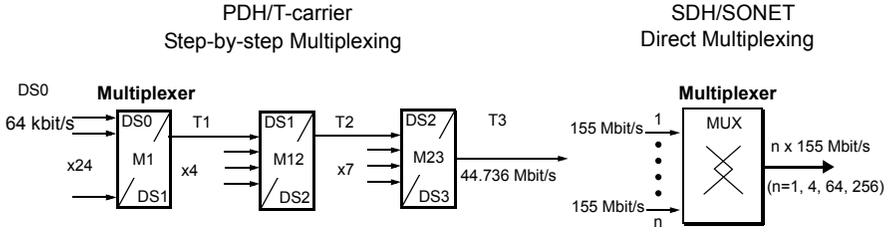


Figure 1.1 SDH and SONET allow for direct multiplexing and demultiplexing.

- Their management, supervision, and maintenance capabilities are limited, as there are no overhead bytes to support these functions. One example of this is that if a resource fails, there is no standard function whereby the network can be reconfigured.
- Access to 64-kbit/s digital channels from higher PDH hierarchical signals requires full demultiplexing, because the use of bit-oriented procedures removes any trace of the channels.
- In PDH it was not possible to create higher bit rates directly; one could do so only after following all the steps and hierarchies (see Figure 1.1).
- Plesiochronous ANSI and *European Telecommunications Standard Institute* (ETSI) hierarchies were not compatible.
- There were no standards defined for rates over 45 Mbit/s in T-carrier, and over 140 Mbit/s in PDH.
- Different manufacturers of plesiochronous equipment could not always be interconnected, because they implemented additional management channels or proprietary bit rates.

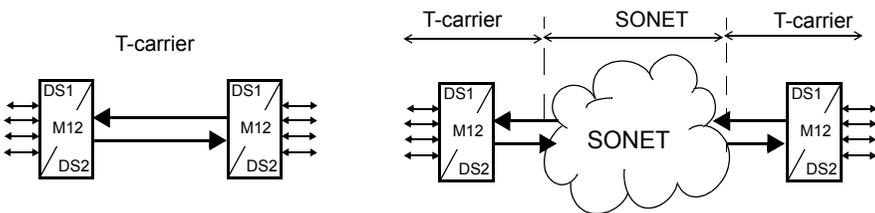


Figure 1.2 SONET and SDH assumed legacy T-carrier and PDH as native transport interfaces. New networks became hybrid, as the interfaces remained plesiochronous while the long-haul transport network was synchronous.

These limitations meant that it was necessary to design a new transmission architecture to increase the flexibility, functionality, reliability, and interoperability of networks.

1.1.2 The SDH/SONET Challenge

What had to be decided first was how to provide smooth migration from legacy installations. Then a basic frame period of $125\ \mu\text{s}$ was selected, the same of E1 and T1 frames, in order to guarantee compatibility with existing services such as *plain old telephone service* (POTS), *integrated services digital network* (ISDN), *frame relay* (FRL) or any $n \times 64\ \text{kbit/s}$ (see Figure 1.2). Note that a byte constantly carried on a $125\text{-}\mu\text{s}$ frame period defines a 64-kbit/s channel. (see Figure 1.3).

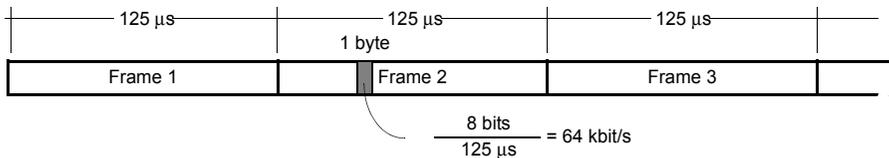


Figure 1.3 SDH frames have a period of $125\ \mu\text{s}$ (8,000 frames per second) and a byte always defines a 64-kbit/s channel, independent of the bit rate.

Some of the remarkable features of SDH compared with its predecessors are:

Synchronous versus plesiochronous

Plesiochronous means “almost synchronous.” This in its turn means that nodes try to do work in the same frequency, but in fact they do not, because each PDH island use its own clock. In *synchronous* networks, all digital transitions should occur simultaneously, and all the nodes must be fed with the same master clock (see Chapter 5). There may, however, be a phase difference between the transitions of the two signals but this must lie within standardized limits.

Bytes versus bits

In SDH and SONET, such basic operations as multiplexing, mapping, or alignment are byte oriented, to keep transported elements identified throughout the whole transmission path (see Figure 1.4).

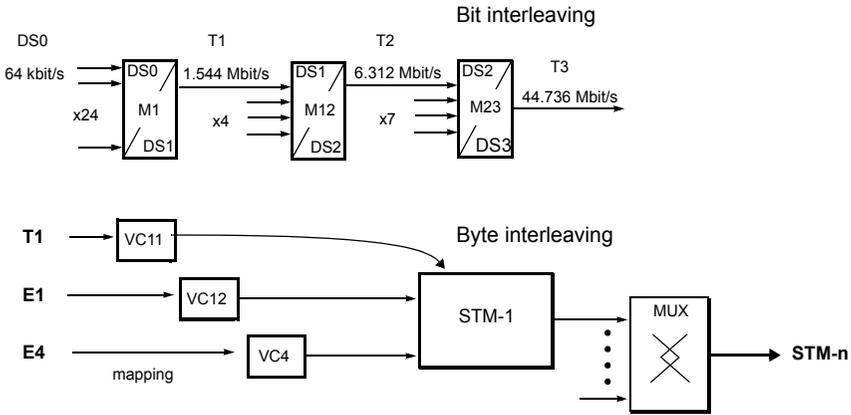


Figure 1.4 SDH multiplexing is based on byte interleaving.

Direct access

The main difference between SDH and its predecessors is in synchronization and byte-oriented operations. Synchronization enables us to insert and extract tributaries directly at any point and at any bit rate, without delay or extra hardware. For this reason, PDH/T-carrier must completely demultiplex signals of various megabits per second, to access any embedded channel of $n \times 64$ kbit/s.

1.1.2.1 Full management

In SDH and SONET, payload and overheads are always accessible, and there is no need to demultiplex the signal. This drastically improves *operation, administration, and maintenance* (OA&M) functions, which are essential to enable centralized management independently of the bit rate.

SDH and SONET also provide embedded mechanisms to protect the network against link or node failures, to monitor network performance, and to manage network events.

1.1.2.2 Providing circuits for public networks

The basic function of SDH, just like any transmission network, is that of providing metropolitan or long-haul transport to networks such as POTS, ISDN, FRL, Gigabit Ethernet (10GbE), *Universal Mobile Telecommunications System* (UMTS) or Internet (see Figure 1.5). Signaling, switching, routing, and billing do not depend on SDH, as it is only in charge of providing bandwidth between two points. (see Figure 1.6).

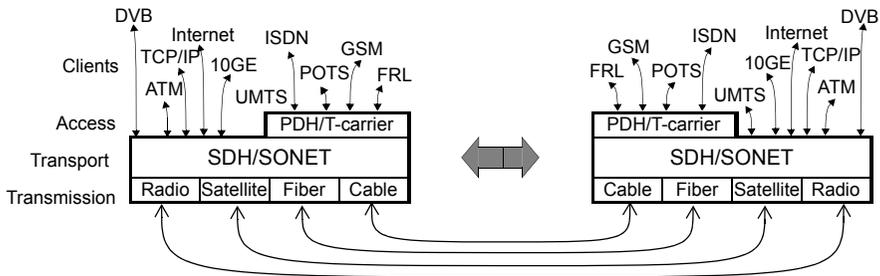


Figure 1.5 SDH and SONET networks offer reliable, efficient, and flexible transport.

1.1.2.3 Universal standard

SDH and SONET standards enable transmission over multiple media, including fiber optics, radio, satellite, and electrical interfaces. They allow internetworking between equipment from different manufacturers by means of a set of generic standards and open interfaces. Scalability is also an important point, as transmission rates of up to 40 Gbit/s have been defined, making SDH a suitable technology for high-speed trunk networks.

1.2 COMPARISON OF SDH AND SONET

SDH and SONET are compatible but not identical. SDH is used worldwide except in the U.S., Canada, Japan, and partially in South Korea, and Taiwan. Both define a similar set of structures and functions; however, there are differences in usage.

Table 1.1
Terminology comparison.

<i>SDH</i>	<i>SONET</i>	<i>SDH</i>	<i>SONET</i>	<i>SDH</i>	<i>SONET</i>
STM-0	OC-1	RSOH	SOH	Regenerator section	Section
STM-X	OC-3X	MSOH	LOH	Multiplex section	Line
AU-3	STS-1	HO POH	STS POH	Higher-order path	STS path
AU-4	STS-3c	F3	Z3	Lower-order path	VT path
AU-4-Xc	STS-3Xc	Z4	K3		
AU-4-Yv	STS-3Yv	LO POH	VT POH		
TU	VT	Z6	N2		
VC	SPE	Z7	K4		

The 51.84-Mbit/s STS-1 is the basic building block of SONET (OC-1 if this signal is transmitted over fiber optics). STS-1 was enough to transport all T-carrier tribu-

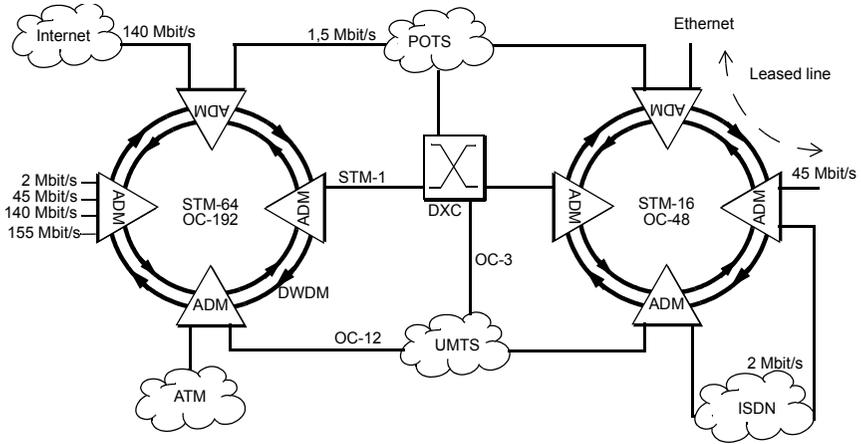


Figure 1.6 The aim of the SDH network is to provide transmission services to other networks.

taries but not to carry the 140Mbit/s PDH tributary. Then SDH chose a basic transport frame three times faster at 155.53 Mbit/s, in order to allocate the full European hierarchy. SDH and SONET terminology have some differences, in referring to the same concepts, bytes, and structures. Nevertheless, beyond the names, the functionality is equivalent (see Table 1.1).

Internetworking is always possible because the evolution of both technologies has been the same with the new hierarchies up to 40 Gbit/s and to the last standards like *link capacity adjustment scheme* (LCAS). The objective is to guarantee universal connectivity.

1.3 FUNCTIONAL ARCHITECTURE

Traditionally, telecommunications networks have been described using a layered model to facilitate their design, implementation, and management. Standardized formats and protocols describe peer interchanges between separate nodes. Interfaces and services define client/server relationships inside each node.

1.3.1 Network Elements

SDH systems make use of a limited number of *network elements* (NEs) within which all the installations are fitted (see Figure 1.7):

- *Regenerators* (REGs) or *section terminating equipments* (STEs): Every signal sent through any transmission medium (optical, electrical or radio-electrical) experiences attenuation, distortion, and noise. Regenerators supervise the re-

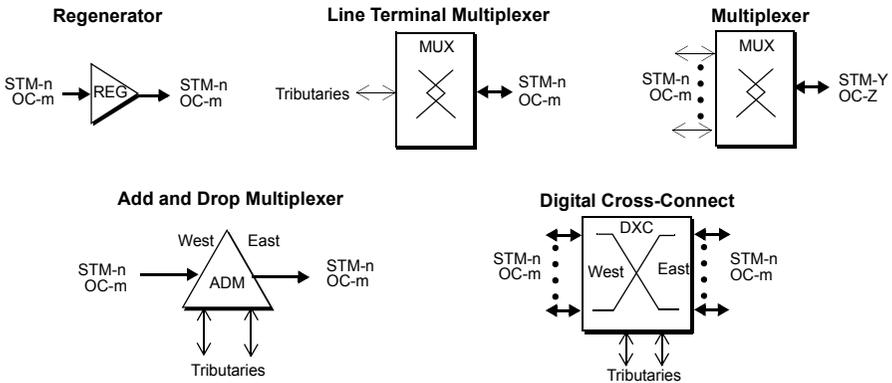


Figure 1.7 SDH network elements (NE).

ceived data and restore the signal’s physical characteristics, including shape and synchronization. They also manage the monitoring and maintenance functions of the *regenerator section* (RS) or *section* in SONET (see Figure 1.10).

- *Line terminal multiplexers* (LTMUX) or *path terminal equipment* (PTE): they are common in line and access topologies. Their function is to insert and extract data in synchronous frames (see Figure 1.10).
- *Add and drop multiplexers* (ADMs) can insert or extract data directly into or from the traffic that is passing across them, without demultiplexing/multiplexing the frame. Direct access to the contents of the frame is a key feature of SDH, as it enables us to turn any point of the network into a service node, just by installing an ADM.
- *Digital cross-connects* (DXCs) configure semipermanent connections to switch traffic between separate networks. The switched traffic can be either SDH streams or selected tributaries. Although it is not common, DXCs can also insert and drop tributaries in transport frames.

1.3.2 Network Topology

Synchronous multiplexers provide great flexibility for building topologies, which is why point-to-point, linear, ring, hub, meshed, and mixed topologies are all possible (see Figure 1.8):

- *Linear point-to-multipoint*: this topology follows the basic point-to-point structure, but now includes ADM multiplexers performing add and drop functions at intermediate points.
- *Ring*: this topology closes itself to cover a specific area, with ADM multiplexers installed at any point. It is flexible and scalable, which makes it very suit-

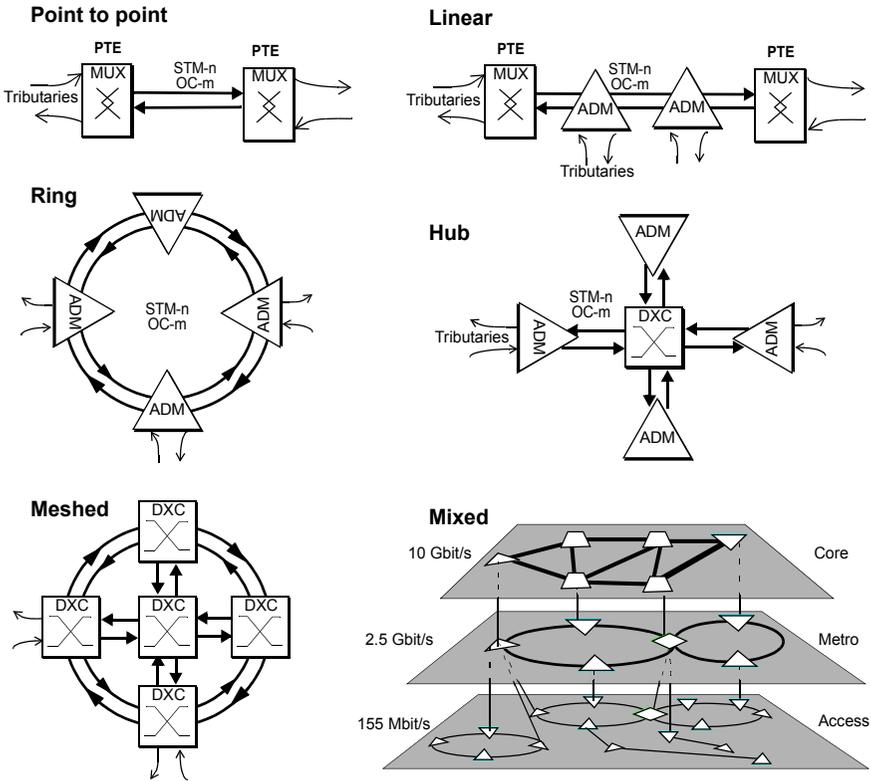


Figure 1.8 Network topologies.

able for wide area and metropolitan networks. Rings are frequently used to build fault-tolerant architectures.

- *Hub or star*: this topology concentrates traffic at a central point, to make topology changes easier. A hub can join several networks with different topologies.

1.3.3 Topology Partitioning

Topology describes the potential connections in a network. Moving from top down, a network can be split repeatedly in interconnected subnetworks. We can describe a subnetwork by means of linked nodes. Nodes are network elements, such as switches, multiplexers, and regenerators. Links can be optical, electrical, and radioelectrical (see Figure 1.10).

1.3.4 SDH/SONET Layers

In plesiochronous networks, interactions are simple and direct. In synchronous networks they are more sophisticated, so responsibilities have been divided among

Formats and Protocols

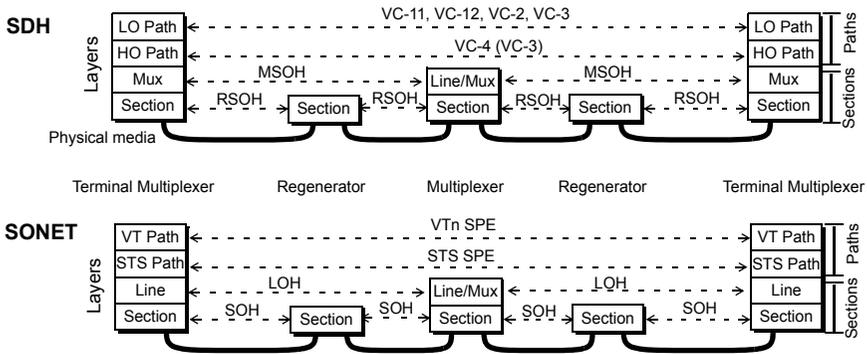


Figure 1.9 SDH and SONET standards define a layered client/server model that can be divided into up to four layers in order to manage transmission services.

several layers that communicate with their counterparts by making use of specific overheads, formats, and protocols. This architecture is equivalent to the layered *open system interconnection* (OSI) model to define and design communication networks (see Figure 1.9).

1.3.4.1 Path layers

Path layers are the route to transport clients' information across the synchronous network from its source to its destination, where the multiplexers interface with client equipment (see Figure 1.9). At this layer clients' information is mapped/demapped into a frame and path overhead is added. There are two specialized path layers (see Figure 1.10):

1. *Lower-order path* (LP), or *virtual tributary path* (VT Path) in SONET, to transport lower-rate services. Associated overhead is *lower-order path overhead* (LO-POH) or *virtual tributary path overhead* (VT-POH) in SONET.
2. *Higher-order path* (HP), *synchronous transport signal path* (STS Path) in SONET, to transport higher-rate services or a combination of lower-rate services. Associated overhead is *higher-order path overhead* HO-POH or *synchronous transport signal path overhead* (STS-POH) in SONET.

Some of the path layer functions are routing, performance monitoring, anomalies and defect management, security and protection, as well as specific path OAM functions support.

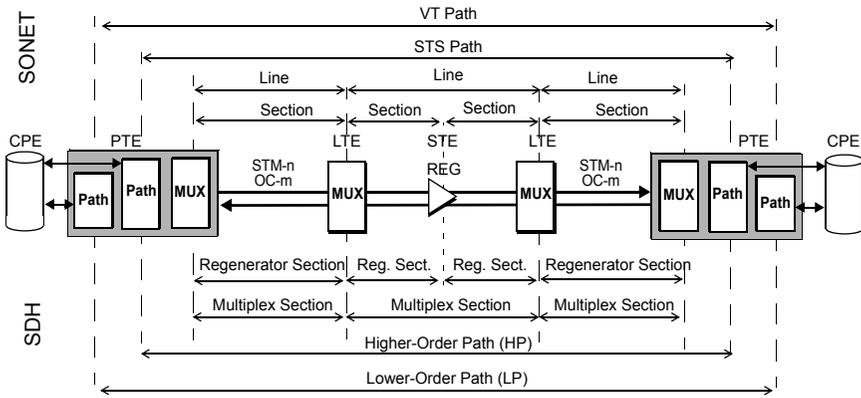


Figure 1.10 SDH and SONET line topology and network layers.

1.3.4.2 Multiplex section or line layer

Multiplexer section (MS), or *line section* in SONET, is a route between two adjacent multiplexers. This layer has several capabilities such as bit error detection, and circuit protection when an intermediate link or node collapses. It also carries synchronization reference information and OAM information between nodes. Associated overhead is *multiplex section overhead (MSOH)* or *line overhead (LOH)* in SONET (see Figure 1.9).

1.3.4.3 Regeneration section or section layer

The regeneration section (RS), (the *section* layer in SONET) is the link between two successive NEs. It reads and writes specific overheads and management functions for each type of transmission media. Its most typical functions are framing, bit error detection, and regenerator OAM functions support. Associated overhead is *regeneration section overhead (RSOH)* or *<Default Para Font>section overhead (SOH)* in SONET (see Figure 1.9).

1.3.4.4 Physical layers

Fiber optics and metallic cable, together with terrestrial radio and satellite links can be used as the *physical layer (PL)*. Fiber optics is the most common medium because of its capacity and reliability. Radio is a cost-effective medium when distance, geographical difficulties, or low-density areas make the optical alternative less practical. Nevertheless, radio has some important weaknesses; for example, noise and frequency allocation, that limit bit rates to 622 Mbit/s. Electrical cables are also used in some legacy installations (see Figure 1.10).

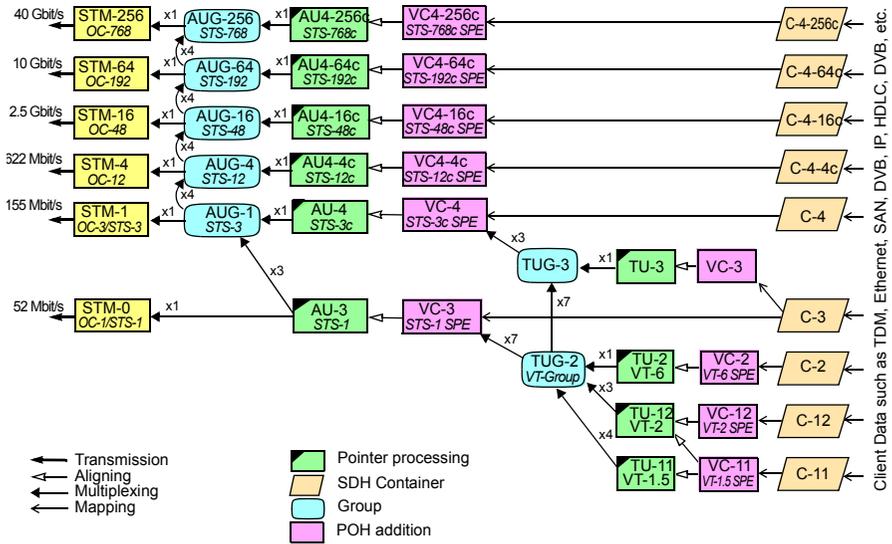


Figure 1.11 SDH and SONET Multiplexing map.

1.4 SDH/SONET FORMATS AND PROCEDURES

SDH defines a set of structures to transport adapted payloads over physical transmission networks (ITU-T Rec. G.707). Five basic procedures are involved here (see Figure 1.11):

- *Mapping:* A procedure by which tributaries are adapted into virtual containers at the boundary of an SDH network.
- *Stuffing:* This is a mapping procedure to adapt the bit rate of client data streams into standardized, fixed-size containers.
- *Multiplexing:* A procedure by which multiple lower-order signals are adapted into a higher-order path signal, or when the higher-order path layer signals are adapted into a multiplex section.
- *Overhead addition:* This procedure is to attach information bytes to a data signal for internal routing and management.
- *Aligning:* A procedure by which a pointer is incorporated into a *tributary unit* (TU) or an *administrative unit* (AU). TU and AU pointers are used to find units anywhere in the transmission network.

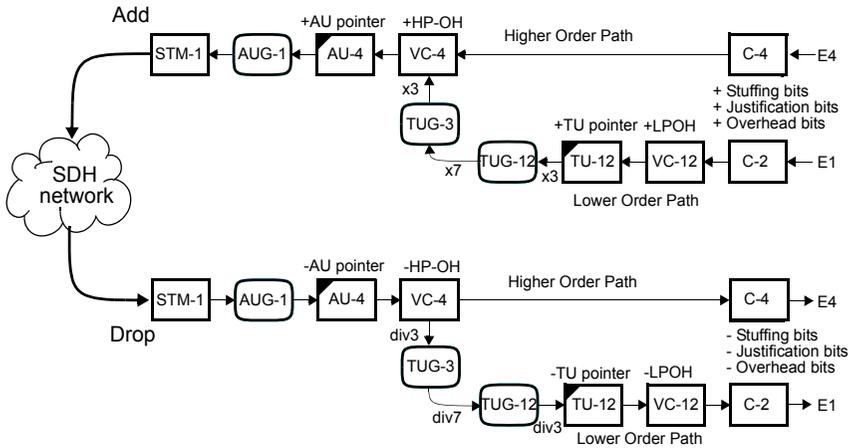


Figure 1.12 Two examples: E4 (140 Mbit/s) and E1 (2 Mbit/s) transport. Transmission and reception operations are symmetrical, and any bit, pointer, or multiplexing performed by the transmission multiplexer is reversed by the receiver multiplexer.

When the tributary reaches the end of the transport network, demapping, demultiplexing, and overhead removal procedures are performed to extract and deliver the tributary (see Figure 1.12).

1.4.1 SDH/SONET Frame Structure

The basic transport frame in SONET is *synchronous transport signal* (STS-1), while in SDH it is *synchronous transmission module* (STM-1) (see Figure 1.13):

- STS-1 is a 3 x 9 byte structure transmitted at 52 Mbit/s, which is equivalent to STM-0.
- STM-1 is a 9 x 9 byte structure transmitted at 155 Mbit/s, which is equivalent to *optical carrier 3* (OC-3) and electrical STS-3.

Both have the same structure that is based on three types of information blocks:

1. *Overhead blocks*: These blocks contain information that is used to manage quality, anomalies, defects, data communication channels, service channels, and so on. There are two types of overhead blocks, RSOH (managed by the regenerator section layer) and MSOH (managed by the multiplex section layer).
2. *Payload blocks* or *virtual containers (VCs)*: They contain a combination of client signals and overhead blocks. VC does not have a fixed position in the frame, but it floats in the frame to accommodate clock mismatches.

3. *Pointers*: They track the VC position, pointing to its first byte, while moving inside the frame (see Figure 1.13).

1.4.1.1 Containers as transport interfaces

Containers (C-*n*) are used to map client bit streams. Adaptation procedures have been defined to suit most telecom transport requirements. These include PDH, *metropolitan area network* (MAN), *asynchronous transfer mode* (ATM), *high-level data link control* (HDLC), *internet protocol* (IP), and Ethernet streams.

Placing signals inside a container requires a stuffing function to match the client stream with the container capacity. The justification function is necessary for asynchronous mappings, to adapt clock differences and fluctuations.

1.4.1.2 Virtual containers or virtual tributaries

Virtual containers (VC-*n*) or virtual tributaries (VTs) in SONET (see Figure 1.14), support end-to-end path layer connections; that is, between the point where the client stream is inserted into the network and the point where it is delivered. Nobody is allowed to modify the VC contents across the entire path.

VCS consist of a C-*n* payload and a *path overhead* (POH). Fields are organized into a block structure that repeats every 125 or 500 μ s. Containers hold client data, and the POH provides information to guarantee end-to-end data integrity.

There are two types of VCs:

- The *lower-order VC*, such as VC-11, VC-12, VC-2, and VC-3¹. These consist of a small container (C-11, C-12, C-2, and C-3), plus a 4-byte POH attached to the container (9 bytes for VC-3).
- The *higher-order VC*, such as VC-3 or VC-4. These consist of either a big container (C-3, C-4) or an assembly of *tributary unit groups* (TUG-2, TUG-3). In both cases, a 9-byte POH is attached.

1.4.1.3 Tributary units and tributary unit groups

A tributary unit is a structure for adaptation between the lower-order and higher-order path layer.

1. VC-3 can be transported through a lower-order path or a higher-order path, depending on the multiplexing map used (see Figure 1.11).

A TUG is an SDH signal made up of byte-interleaved multiplexing of one or more TUs. In other cases, lower-order TUGs are multiplexed to form a higher-order TUG (for instance, seven multiplexed TUG-2s form one TUG-3), and in other cases, a TUG is formed by a single TU (for instance, a single TU-3 is enough to form a TUG-3). TUGs occupy fixed positions in higher-order VCs.

1.4.1.4 Administrative unit

An administrative unit (AU-*n*) provides adaptation between the higher-order path layer and the multiplex section layer. It consists of an HO-VC payload and an AU pointer indicating the payload offset.

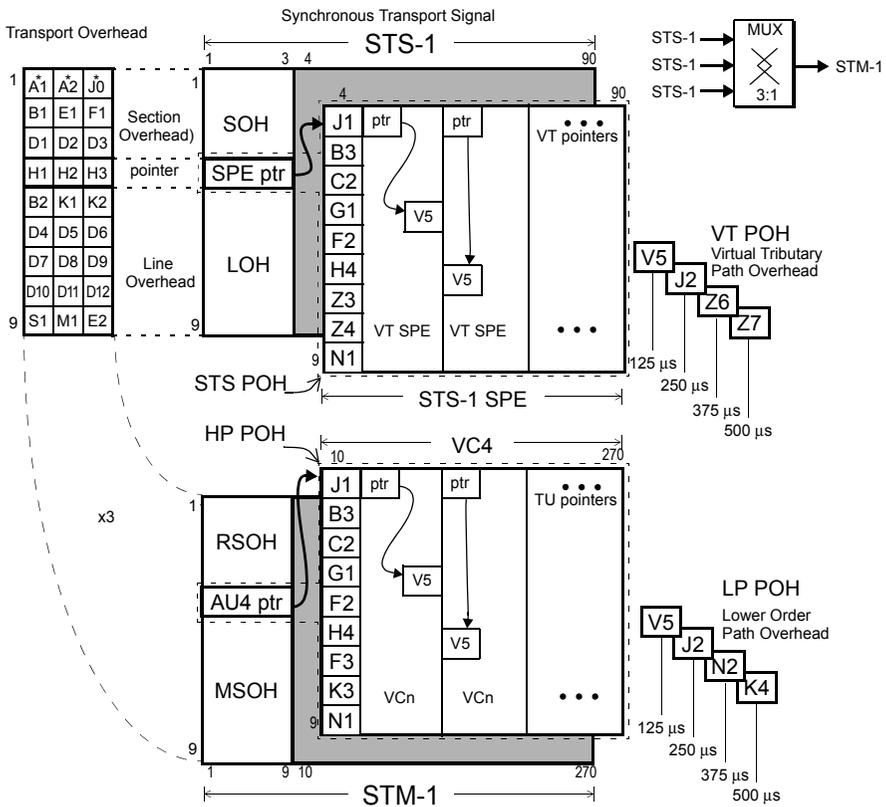


Figure 1.13 SONET and SDH differences are minimal, both are highly compatible, and most differences fall into certain names and acronyms. SDH-to-SONET gateways need to adapt just a few bytes. In the figure, the STS-1 and STM-1 represent the basic frames of SONET and SDH.

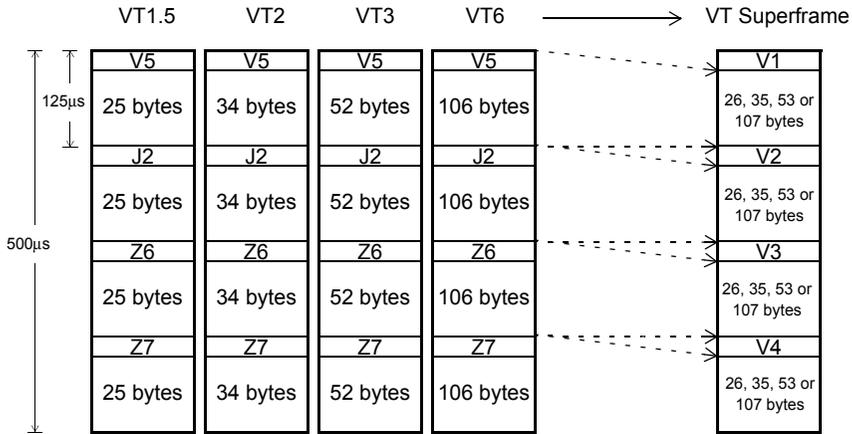


Figure 1.14 SONET virtual tributary superframes.

1.4.2 Multiplexing Map

A multiplexing map is a road map that shows how to transport and multiplex a number of services in STM/OC frames (see Figure 1.11).

- The client tributary (PDH, T-carrier, ATM, IP, Ethernet, etc.) needs to be mapped into a C-*n* container, and a POH added to form a VC-*n*, or a VT for SONET.
- The VC/VT is aligned with a pointer to match the transport signal rate. Pointers together with VCs form TUs or AUs.
- A multiplexing process is the next step, whereby TUG-*n* and AUG-*n* groups are created.
- When it comes to TUGs, they are multiplexed again to fill up a VC, *synchronous payload envelope* (SPE) in SONET, and a new alignment operation is performed.
- Finally, an *administrative unit group* (AUG) is placed into the STM/OC transport frame.

1.5 SDH TRANSPORT SERVICES

Today’s telecommunications services (voice, data, TV, Internet) are heterogeneous, based on a diverse combination of technologies. Most of them are clients of SDH when they need to extend their service range to wider areas.

Channelized networks in 64-kbit/s circuits (POTS, ISDN, FRL, GSM, FRL) are mapped transparently in SDH synchronous containers designed to transport PDH or T-carrier tributaries. Packet technologies, such as IP, Ethernet or ATM, also have special mapping procedures (see Figure 1.6).

Table 1.2
VC types and capacity.

<i>SDH</i>	<i>SONET</i>	<i>Bandwidth</i>	<i>Payload</i>
VC-11	VT 1.5 SPE	1,664 kbit/s	1,600 kbit/s
VC-12	VT 2 SPE	2,240 kbit/s	2,176 kbit/s
VC-2	VT 6 SPE	6,848 kbit/s	6,784 kbit/s
VC-3	STS-1 SPE	48,960 kbit/s	48,384 kbit/s
VC-4	STS-3c SPE	150,336 kbit/s	149,760 kbit/s
VC-4-4c	STS-12c SPE	601,344 kbit/s	599,040 kbit/s
VC-4-16c	STS-48c SPE	2,405,376 kbit/s	2,396,160 kbit/s
VC-4-64c	STS-192c SPE	9,621,504 kbit/s	9,584,640 kbit/s
VC-4-256c	STS-768c SPE	38,486,016 kbit/s	38,338,560 kbit/s

PDH/T-carrier over SDH

To guarantee smooth migration from legacy installations, SDH standards have defined procedures to transport all legacy circuits (E1, E2, E3, E4, T1, T2, and T3). This way, all former PDH/T-carrier services (ISDN or FRL) are today transported by hybrid PDH/SONET or T-carrier/SONET networks.

- Synchronous mapping maintains the original 64-kbit/s channel structure during the whole transmission, making it possible to access these channels directly, as bit justification is not needed. This is common in such services as ISDN or FRL, where there are nodes synchronized with the SDH reference clock. Small clock differences are adjusted with pointer movements.
- Asynchronous mapping is used when PDH and SDH do not share the same clock. Here we need bit-oriented justification to adjust any clock differences between the PDH signal and the SDH container. Due to this, the existing byte structure is lost. This scheme is rather common in POTS and in old plesiochronous circuits.

ATM over SDH

ATM cells are mapped into containers at different bit rates. The range goes from a few Mbit/s up to several Gbit/s, using any concatenation technique (see Section 1.9).

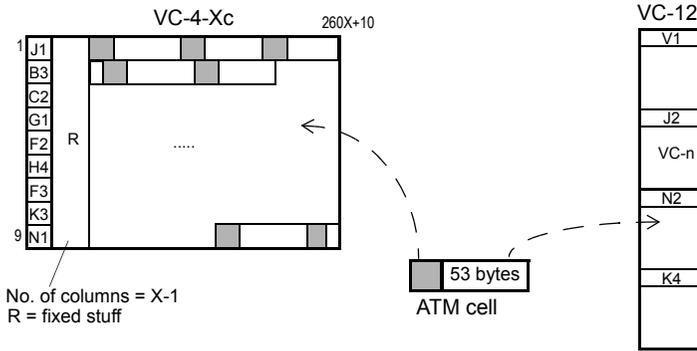


Figure 1.15 Mapping ATM cells in VC-n and concatenated VC-4-Xc.

ATM cells are mapped by aligning every cell with the structure of virtual or concatenated containers. Since capacity may not be an integer multiple of the ATM cell length (53 bytes), a cell is allowed to cross the container frame boundary (see Figure 1.15). The ATM cell information field (48 bytes) is scrambled before mapping, to guarantee delineation. An ATM cell stream with a data rate that can be mapped is equal to the VC payload capacity (see Table 1.2).

Mapping HDLC-framed signals

HDLC-framed signals are mapped by aligning the byte structure of every frame with the byte structure of the VC. The range also goes from 1.5 Mbit/s up to several Gbit/s using concatenation techniques (see Section 1.9). 7Ex HDLC flags are used between frames to fill the buffer, due to the discontinuous arrival of HDLC-framed signals. Since HDLC frames are of variable length, a frame may cross the container boundary.

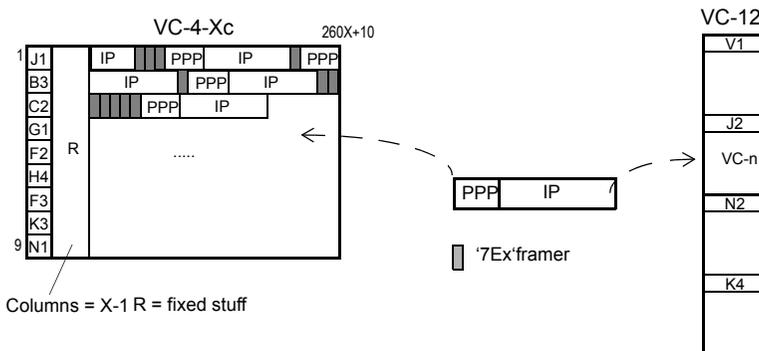


Figure 1.16 Mapping HDLC frames enables IP transport.

Packet over SDH

Packet over SDH (PoS) enables core routers to send native IP packets directly over SDH container frames, using *point to point protocol* (PPP) for framing and bit error detection. The *request for comments 2615* (RFC 2615) defines the use of PPP encapsulation over SDH circuits.

IP traffic is treated as a serial data stream that travels hop by hop through the network. At each node, IP packets are unwrapped from the PPP frame, destination addresses are examined, routing paths are determined, and, finally, packets are re-wrapped in a new PPP frame and sent on their way (see Figure 1.16).

PoS is more reliable and has lower overhead than its alternatives, such as ATM or frame relay encapsulation.

Ethernet over SDH

Ethernet has become the standard technology for *local area networks* (LANs). It is cheap, easy to use, well-known, and always in constant evolution toward higher rates. Now it is also being considered as a good technology for access and metro networks, but carriers still need SDH to route high volumes of Ethernet traffic to get long haul. There are several schemes:

- *Ethernet over LAPS*: defined in ITU-T X.86. This is an HDLC family protocol, including performance monitoring, remote fault indication, and flow control. However, it calls for contiguous concatenated bandwidth techniques (see Section 1.9) that do not match the burst nature of Ethernet.
- *Generic framing procedure (GFP)*: defined in ITU-T Rec. G.7041. This is a protocol for mapping any type of data link service, including Ethernet, *resilient packet ring* (RPR), and *digital video broadcasting* (DVB).
- *Virtual concatenation*: defined in ITU-T Rec. G.707, creates right-sized pipes for the traffic, providing quite a lot of flexibility and high compatibility with legacy SDH installation techniques.
- *Link capacity adjustment scheme (LCAS)*: defined in ITU-T Rec. G.7042. This dynamically allocates/deallocates new bandwidth to match Ethernet requirements in a flexible and efficient way. It calls for virtual concatenation.

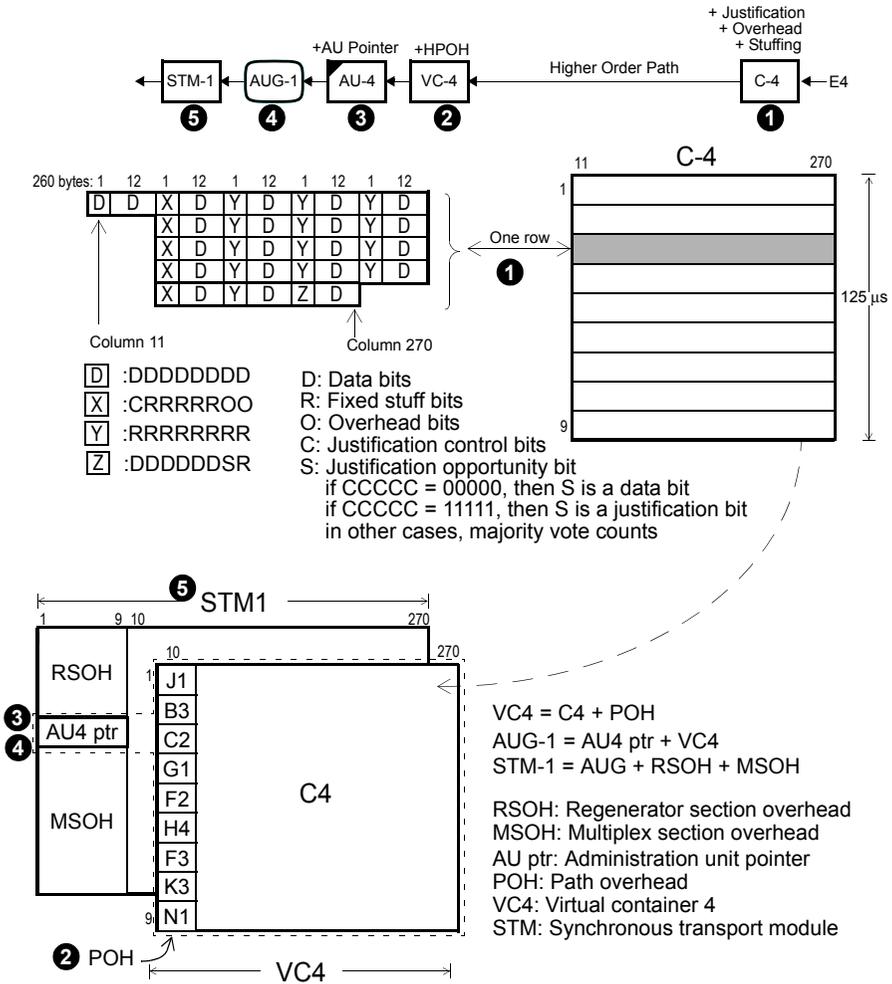


Figure 1.17 Asynchronous mapping of 139,264 kbit/s into a VC-4 and STM-1 frame.

1.6 TRANSPORTING PDH/T-CARRIER TRIBUTARIES

Transporting tributaries always calls for a set of operations (mapping, aligning, multiplexing, etc.) before inserting data into STM-*n*/OC-*m* frames. The number and type of operations may vary, depending on the tributary rate (see Figure 1.11). For higher bit rates (45 or 140 Mbit/s), the operation is straightforward; basically, a mapping process followed by aligning (see Figure 1.17). For lower rate tributaries,

several multiplexing operations are also needed, to fill up the whole STM-*n*/OC-*m* frame capacity (see Figure 1.19).

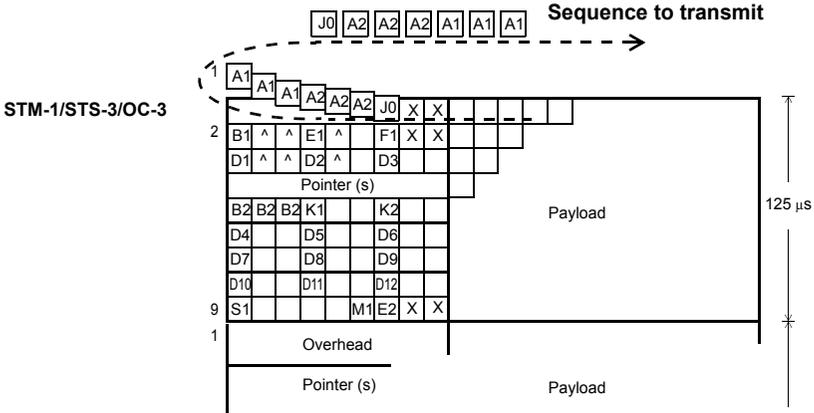


Figure 1.18 STM and STS frames are prepared for serial transmission every 125 μs.

1.6.1 Transport on VC-4 or STS-3c SPE

In a VC-4 container, several client signals can be mapped, including PDH/T-carrier circuits, HDLC-like protocols, and ATM cells (see Figure 1.19). In our example we will look at 140Mbit/s mapping, to describe this in detail:

1. The mapping operation in C-4, whereby a 140 Mbit/s bit stream is fitted into a nine row container. Each row has a justification bit opportunity, so mapping is asynchronous, as PDH circuit itself is asynchronous and does not have a byte-oriented structure.
2. Creation of VC-4 when higher-order path overhead (HO-POH) is added. HO-POH provides end-to-end management and performance monitoring.
3. Alignment or an AU-4 pointer addition, which enables locating the VC-4 floating in the STM-1 frame. AU-4 always points to the first VC-4 byte.
4. A unitary multiplexing operation to create an AUG-1.
5. Adding MSOH and RSOH overheads to build the STM-1 frame.

Now the STM-1 frame is ready to be sent (see Figure 1.18). On reception, in order to deliver the 140-Mbit/s tributary, we must perform these same operations—from 5 to 1.

1.6.2 Transport on VC-3

In a VC-3 container several client signals can be mapped, including PDH/T-carrier circuits, HDLC-like protocols, and ATM cells. Here, we will look at the 45-Mbit/s and 34-Mbit/s transport; in both cases all procedures except mapping are identical.

VC-3 has two transport schemes: (a) Lower-order (LO) transport, where VC-3s are allocated directly into the STM-1 frame; (b) Higher-order (HO) transport, where VC-3s are multiplexed into a VC-4 which is finally placed into the STM-1.

Higher-order transport

The operations and steps to follow are depicted in Figure 2.19:

1. The mapping operation in C-3. The 45 Mbit/s transport uses a one-row structure, while for 34 Mbit/s, three rows are repeated three times.
2. A higher-order path overhead (HO-POH) addition to create a VC-3.
3. An alignment or an AU-3 pointer addition to locate the VC-3.
4. A unitary multiplexing operation to create an AUG-1.
5. Adding MSOH and RSOH overheads to build an STM-1 frame.

Now the STM-1 frame is ready to be sent. On reception, to deliver the tributary, we must perform the same operations vice versa; that is, from 5 to 1.

Lower-order transport

The operations and steps to follow are depicted in Figure 2.19:

1. Mapping is identical to that of higher-order transport.
- b. A lower-order path overhead (LO-POH) addition to form a VC-3.
- c. An alignment operation or AU-3 pointer addition to locate the VC-3. The new structure is called TU-3.
- d. Multiplexing of three different TU-3s to create a TU-3 Group (TUG-3)
- e. Adding an HO-POH to produce a VC-4.
- f. A new alignment operation to find the VC-4.
- g. A unitary multiplexing operation to create an AUG-1.
- h. Adding MSOH and RSOH overheads to build an STM-1 frame.

The STM-1 frame is now ready to be sent. Again, to deliver the tributary, the same operations must be performed vice versa, from 8 to 1, on reception.

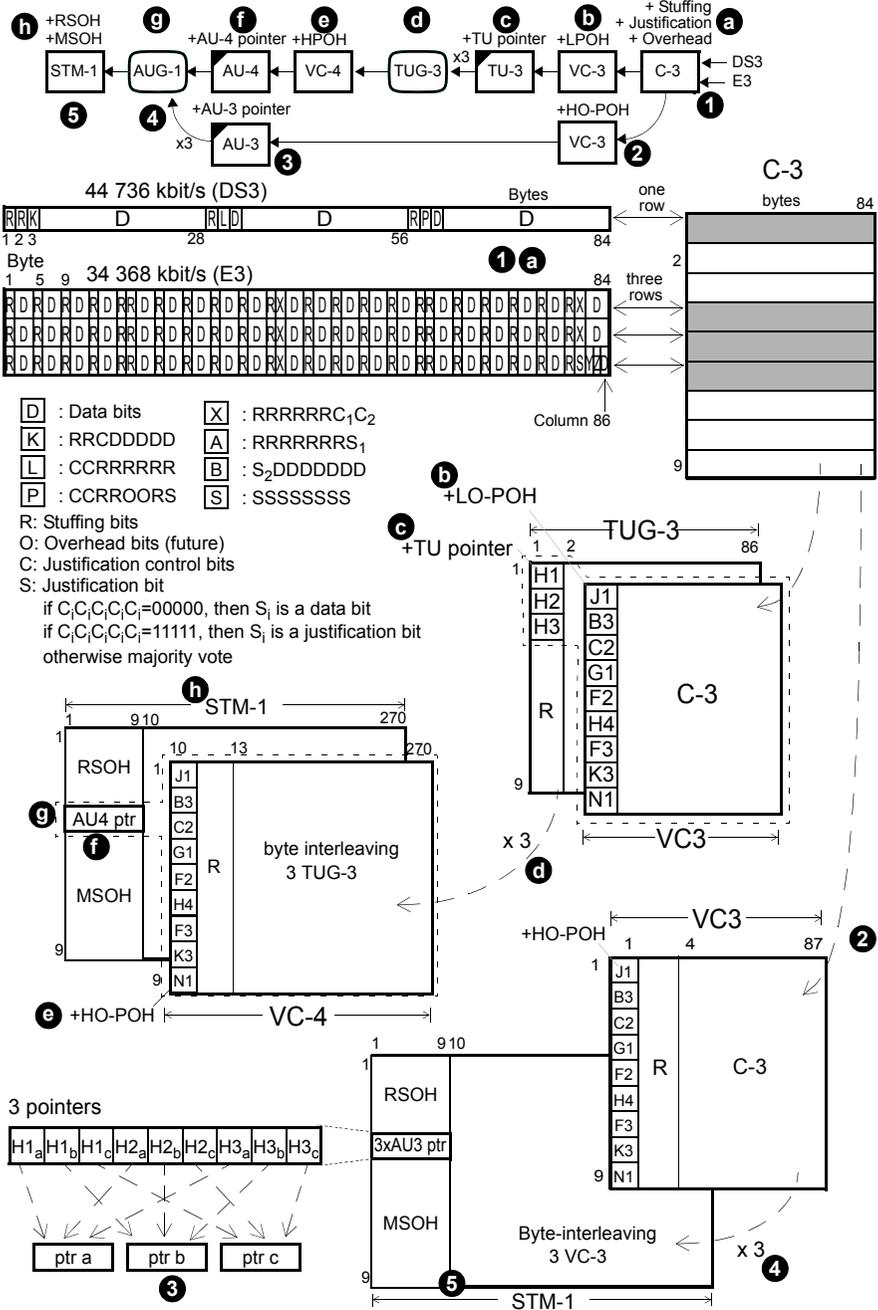


Figure 1.19 Asynchronous mapping of 44,736 kbit/s and 34,368 kbit/s into VC-3 via AU-4 and also via AU-3.

Note that transporting VC-3 via AU-3 calls for three AU-3 pointers in the STM-1 frame. Pointer bytes appear interleaved in the space assigned for them in the structure of the synchronous transport module. In the case of VC-3 transport via AU-4, the first pointer indicates the beginning of the VC-4, and, inside the VC-4 payload, a second level of pointers is needed to locate VC-3 containers.

1.6.3 Transport of 2-Mbit/s Circuits

Transporting 2 Mbit/s can be synchronous or asynchronous. Synchronous mapping is possible only if PDH and SDH networks use the same reference clock. In this case, mapping has certain advantages because it is byte oriented, which means that the 64-kbit/s frame structure of the tributary will be maintained throughout the whole transport, allowing direct access from SDH premises to the voice or data channel.

This does not happen in asynchronous mapping, as it has to use bit-oriented justification mechanisms that break the E1 frame structure. Except for mapping, the operation sequence for both cases is similar (see Figures 2.20 and 2.21):

1. The mapping operation in container C-12. If asynchronous mapping is used, C-12 adopts a 500- μ s multiframe format.
2. Adding lower-order path overhead to create VC-12.
3. Alignment or a TU pointer addition to indicate VC-12 offset. TU-2 is created this way.
4. Multiplexing of three TU-12s, which creates a TUG-2.
5. Multiplexing of seven TUG-2s, which creates a TUG-3.
6. A new multiplexing operation of three TUG-3s plus a HO-POH, together form a VC-4.
7. Alignment or an AU-4 pointer addition enables us to locate the VC-4.
8. A unitary multiplexing operation to create an AUG-1.
9. Adding MSOH and RSOH overheads to build an STM-1 frame.
10. Since VC-12 is a multiframe, then transmission is a four STM-1 multiframe operation (see Figure 1.22).

The STM-1 frame can now be sent. On reception, to deliver the 2-Mbit/s circuit, we must again perform these operations vice versa, from 9 to 1. Note the VC-4 capacity up to 63 x 2 Mbit/s circuits can be transported simultaneously.

At the reception end, to locate each circuit, we must first find the VC-4 using the AU-4 pointer and then, by reading the TU-12 pointer, it is possible to find the VC-12 offset.

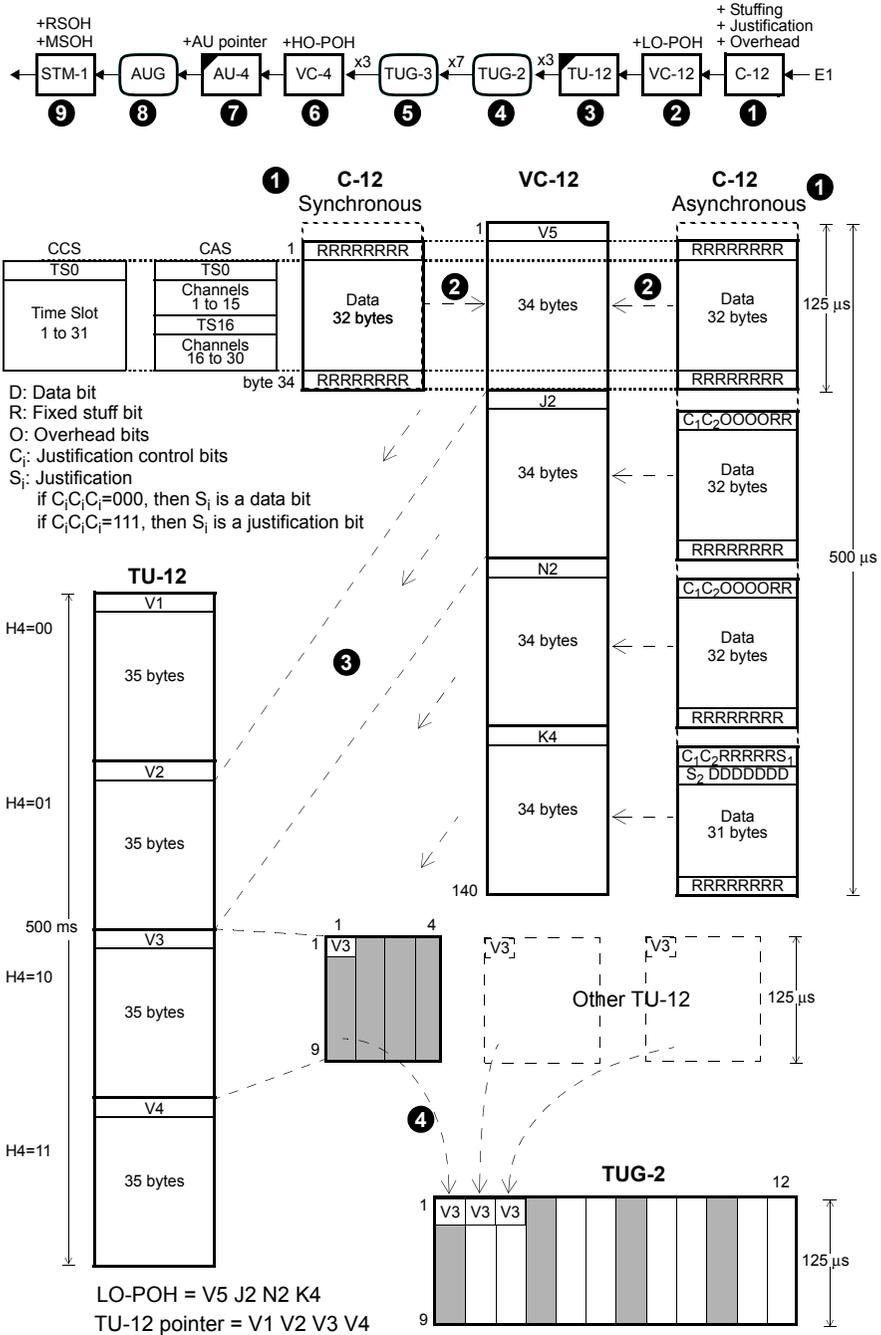


Figure 1.20 Synchronous and asynchronous transport of a 2-Mbit/s circuit (I).

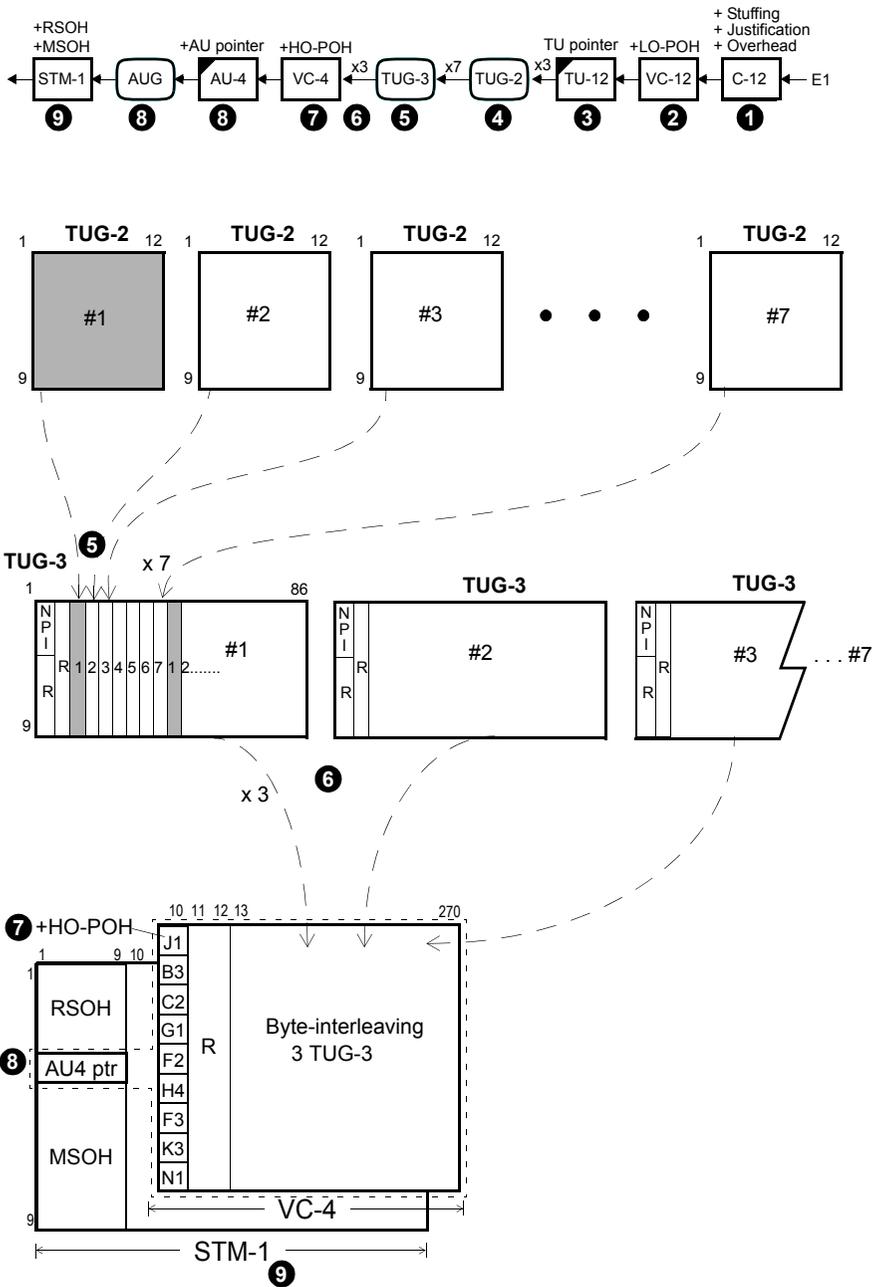


Figure 1.21 Synchronous and asynchronous transport of a 2-Mbit/s circuit (II).

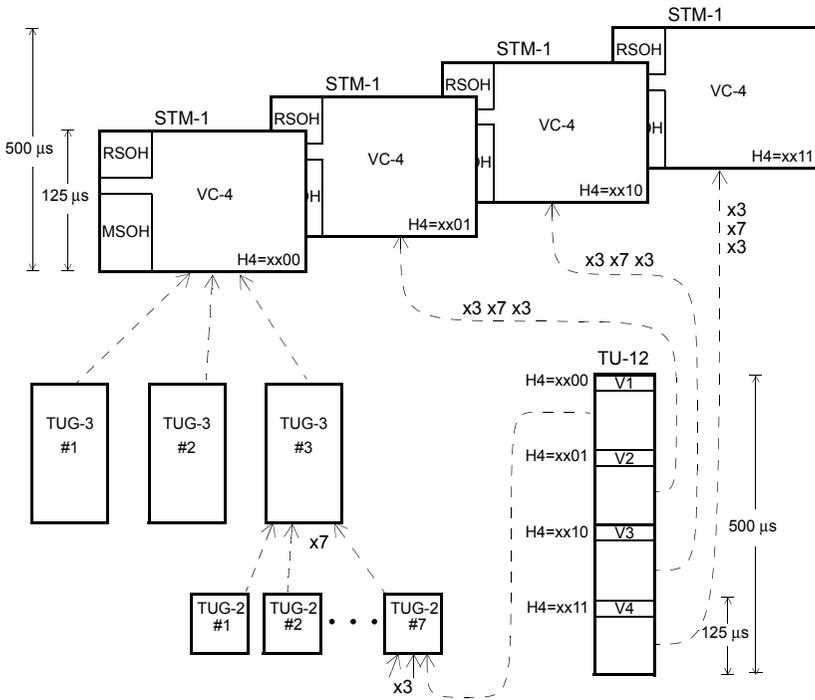


Figure 1.22 VC-12 needs 4 x 125 μs intervals for full mapping. This means that a full VC-12 extends to cover four STM-1 frames.

1.7 POINTERS AND TIMING COMPENSATION

SDH supports two types of timing mismatches: asynchronous tributaries, and time variations of NE clocks. Justification bits are used to compensate differences with tributaries during the mapping operation (see Section 1.6). Pointer adjustments are necessary to compensate slight clock differences of the synchronous equipment (basically ADM and DXC).

1.7.1 Payload Synchronization

Pointers allow for dynamic alignment of the payload within transmission frames. These are necessary, as payloads are floating within the frame to compensate for clock phase fluctuations between NEs (see Figure 1.23).

At this point, we come across a paradox: If SDH is based on node and signal synchronization, why do fluctuations occur? The answer lies in the practical limita-

tions of synchronization. SDH networks use high-quality clocks feeding network elements. However, we must consider the following:

- A number of SDH islands use their own reference clocks, which may be nominally identical, but never exactly the same.
- Cross services carried by two or more operators always generate offset and clock fluctuations whenever a common reference clock is not used.
- Inside an SDH network, different types of breakdown may occur and cause a temporary loss of synchronization. When a node switches over to a secondary clock reference, it may be different from the original, and it could even be the internal clock of the node.
- Jitter and wander effects (see Chapter 5).

1.7.2 Pointer Formats and Procedures

Although pointers have different names (AU-4, AU-3, TU-3, TU-2, TU-1, STS ptr or VT ptr), they all share the same format and procedures (see Figure 1.24):

- Two bytes allocate the pointer (H1-H2 or V1-V2) that indicates the first byte of the payload (see Table 1.3).
- The pointer value 0 indicates that the payload starts after the last H3 or V3 byte.
- Each pointer has its valid range of values.
- The offset is calculated by multiplying n times the pointer value, and n depends on the payload size.

Table 1.3
SDH and SONET pointers.

<i>SDH</i>	<i>Payload</i>	<i>SONET</i>	<i>Payload</i>	<i>Allocation</i>	<i>Range</i>	<i>Hops</i>	<i>Justification</i>
AU-4	VC-4	STS-3 ptr	STS-3c	H1, H2	0 - 782	3 bytes	3 bytes
AU-3	VC-3	STS-1 ptr	STS-1	H1, H2	0 - 782	3 bytes	1 bytes
TU-3	VC-3	—	—	H1, H2	0 - 764	1 byte	1 byte
TU-2	VC-2	VT-6 ptr	VT-6	V1, V2	0 - 427	1 byte	1 byte
TU-12	VC-12	VT-2 ptr	VT-2	V1, V2	0 - 139	1 byte	1 byte
TU-11	VC-2	VT-15 ptr	VT-15	V1, V2	0 - 103	1 byte	1 byte

1.7.2.1 Pointer Generation

In normal operation, pointers are located at fixed positions, and the *new data flag* (NDF) is 0110. However, sometimes it is necessary to change the pointer value, in which case the following rules apply:

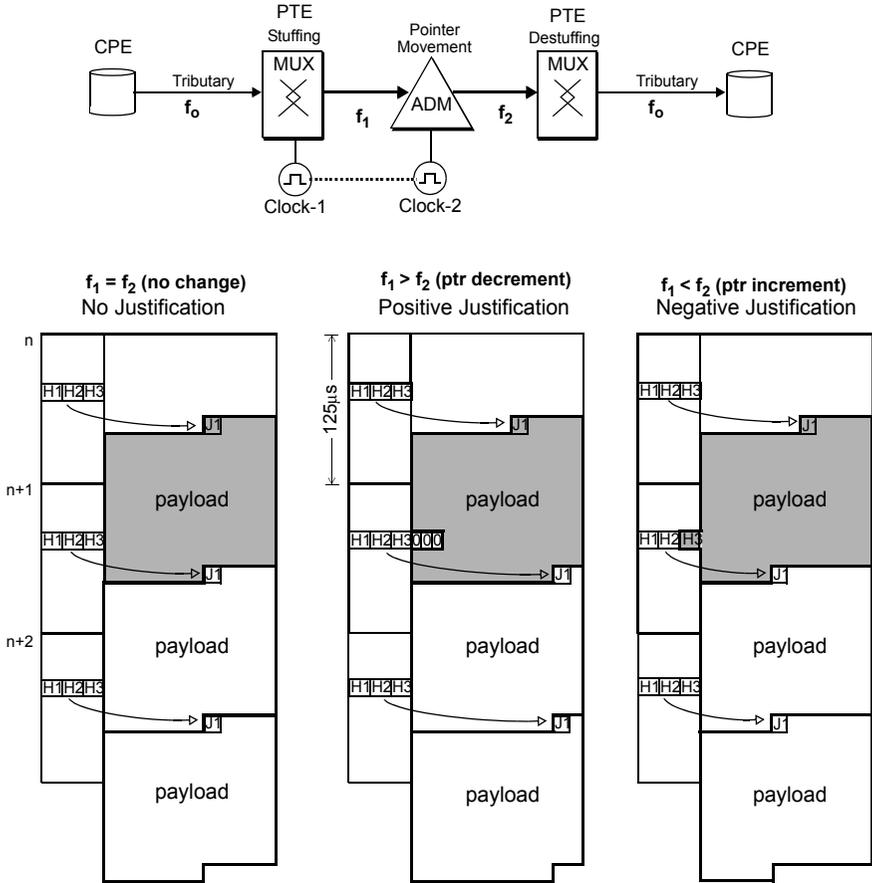


Figure 1.23 The pointer adjustment operation used by LTE to compensate for clock mismatch. Consecutive pointer operations must be separated by at least 500 µs.

- *Minimum time period:* The minimum time period between two consecutive pointer changes is 500 µs.
- *Pointer increment:* If a positive justification is required, the pointer value is sent with the I-bits inverted. The new pointer value is the previous value, incremented by one. If the pointer is H1-H2, the position of the payload is shifted three bytes forward, and void bytes are left after H3. If it is V1-V2, the payload is shifted one byte forward, and a void byte is left after V3.
- *Pointer decrement:* If a negative justification is required, the pointer value is sent with the D-bits inverted. In this case, the new pointer value is the previous value decremented by one. If the pointer is H1-H2, the position of the payload

is shifted three bytes backwards, and H3 provides spare bytes. If the pointer is V1-V2, the payload is shifted one byte backwards, and either V3 provides the spare byte.

- *New pointer:* If the VC-n alignment changes for any reason, and it cannot be tracked by pointer increments or decrements, then a new pointer value is sent, and the NDF is set to 1001 to reflect the new value.

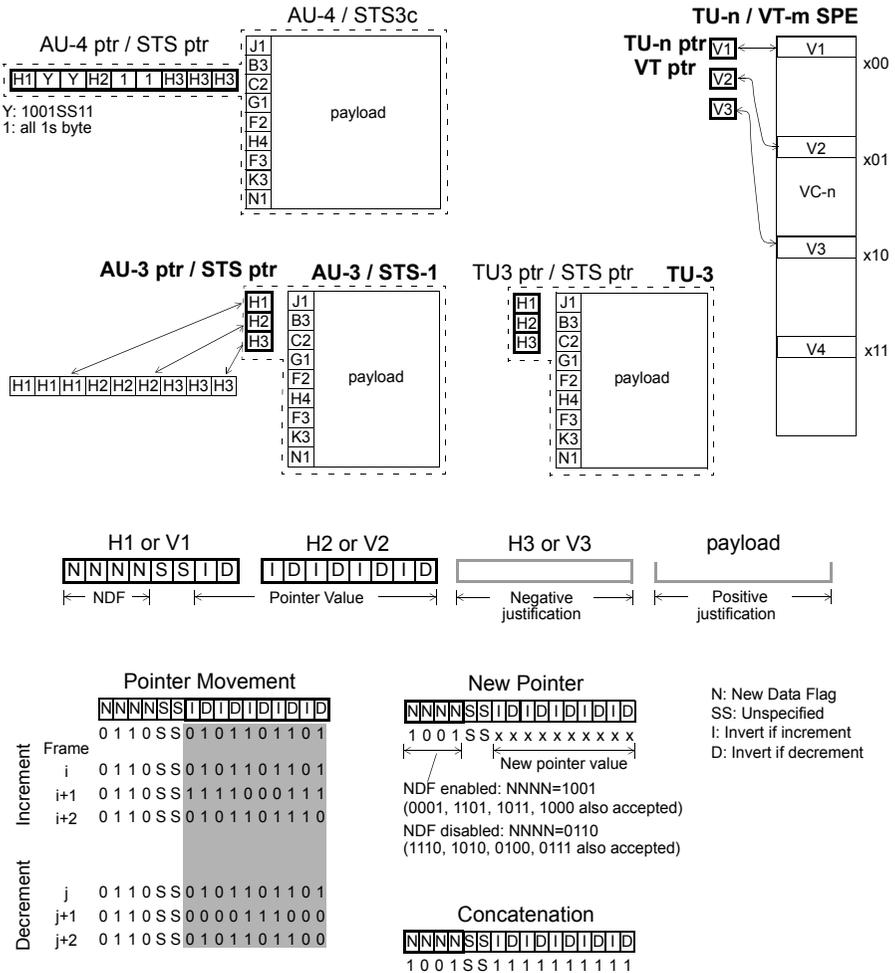


Figure 1.24 Pointer formats, codification, and procedures.

1.8 OVERHEADS

The key difference between SDH and its plesiochronous predecessors is in the management and monitoring capabilities SDH provides at the transmission layer. These features are based on peer protocols, standardized formats, and overhead fields. Network elements themselves generate a suitable response to management actions, reconfigurations, performance monitoring, failures, or any type of events. Overheads are also a key difference between SDH and its potential successors, based on any combination of *gigabit-Ethernet* (GbE), *dense wavelength division multiplexed* (DWDM), and IP protocols. These networks are always said to be more efficient, because they do not support most of these management facilities and, eventually, will not need overheads or protocols to support them.

Table 1.4
Nine-byte path overhead for VC-3, VC4, VC-4-Xc, STS-1 SPE, and STS-Xc SPE.

Byte	Description
J1	<i>HP trace:</i> Its position is indicated by the AU- <i>n</i> or the TU-3 pointer. It carries a configurable sequence identifier of 16 or 64 bytes (including a CRC-7 byte), so that the receiving path terminal can continuously verify its connection with the transmitter.
B3	<i>HP error monitoring:</i> This is a bit interleaved parity 8 (BIP-8) code using even parity, computed over all bits of the previous VC-3, VC-4, or VC-4-Xc before scrambling.
C2	<i>Path signal label:</i> This indicates the composition or mapping of the VC- <i>n</i> . 0x: Unequipped, 01x: Reserved, 02x: TUG structure, 03x: Locked TU- <i>n</i> , 04x: 34-Mbit/s or 45-Mbit/s mapping, 12x: 140-Mbit/s mapping, 13x: ATM mapping, 14x: <i>distributed queue dial bus</i> (DQDB) mapping, 15x: <i>fiber distributed data interface</i> (FDDI) mapping, 16x: HDLC/PPP mapping, 17x: <i>simple data link</i> (SDL) mapping, 18x: Mapping of HDLC/LAPS, 19x: SDL mapping, 1Ax: 10 GbE, 1Bx: GFP mapping, CFx: Obsolete mapping of HDLC/PPP, from E1x to FC: reserved for national use, FEx: test signal O.181.
G1	<i>HP status and performance:</i> This byte enables continuous monitoring of anomalies and defects either at path end or at any point along the trail. Bits 1-4: remote error indication (HP-REI) conveys the number of bit errors detected by B3. Bit 5: remote defect indication (HP-RDI), is sent back if a signal failure is detected. Bits 6-7 can be used to provide enhanced RDI information to differentiate between payload defects (HP-PLM), server defects (HP-AIS, LOP), and connectivity defects (HP-TIM, HP-UNEQ).
F2, F3	<i>HP user channel:</i> User communication purposes between path terminations.
H4	<i>Sequence indication for virtual VC-3/4 concatenation:</i> If the payload is VC-2, VC-12, or VC-11, it is used as a multiframe indicator.
K3 _(bit1-4)	<i>APS signaling:</i> Allocated for the VC-3/4 protection protocol in case of a failure
K3 _(bit7-8)	HP data communication channel of 16 kbit/s.
N1	<i>HP tandem connection monitoring function (HP-TCM):</i> Two options are described in the G.707 (Appendix C and D). Bits 1-4: incoming error count (IEC), bit 5: TC remote error indication (TC-REI), bit 6: outgoing error indication (OEI), bits 7-8: operate in a 76-byte multiframed string including access point identifier (TC-APId), a generic 16-byte identifier, and a remote defect indication (TC-RDI).

Nine-byte Path Overhead (POH)

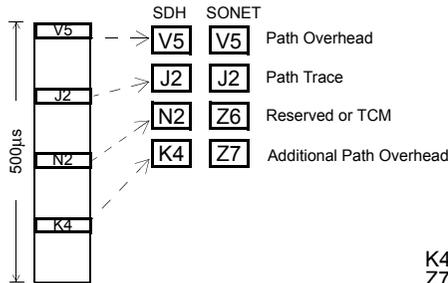
SDH	SONET	
J1	J1	Path trace, message with CRC
B3	B3	BIP-8 parity control
C2	C2	Signal label (mapping)
G1	G1	Path status
F2	F2	Path user channel (voice or data)
H4	H4	Position and sequence indicator
F3	F3	Path user channel (voice or data)
K3	Z3	Automatic Protection Switch
N1	Z4	Tandem Connection Monitoring

C2:	00: Unequipped	14: DQDB
	01: Reserved	15: FDDI
	02: TUG	16: HDLC/PPP
	03: Locked TU	17: SDL
	04: E3, T3	18: HDLS/LAPS
	12: E4	1A: 10GbEthernet
	13: ATM	FE: Test Signal

K3:	APS	HODL	Spare
Z3:			

APS: Automatic Protection
HODL: Higher Order Data Link

Four-byte Path Overhead (POH)



N2:	multiframe					
Z6:	BIP-2	1	I-AIS	TC-REI	OEI	TC-API, TC-RDI, ODI, reserved

BIP2 for Tandem Connection calculated over the VC
I-AIS: Incoming AIS
TC-REI: Remote Indication Error in a TC subnetwork
OEI (Outgoing Error Indication)
Multiframe: TC-API (Access Point Identifier)
(76 frames)TC-RDI (RDI in Tandem Connection)
ODI (Outgoing Defect Indication)

G1:	REI	RDI	E-RDI	Spare
-----	-----	-----	-------	-------

REI (Remote Error Indication) BIP-8 violation count
RDI (Remote Defect Indication) is sent back
E-RDI (Enhanced RDI information)
(RDI=0) 10: Payload defect (PLM)
(RDI=1) 01: Server defect (AIS, LOP),
(RDI=1) 10: Connectivity defect (TIM, UNEQ)

N1:	multiframe				RDI
Z4:	IEC	TC-REI	OEI	TC-API, TC-ODI, reserved	

IEC Incoming Error Count, BIP-8 errors in Tandem Conn.
TC-REI: Remote Error Indication in a TC subnetwork
OEI: Outgoing Error Indication
Multiframe: TC-API (Access Point Identifier)
(76 frames)TC-RDI (RDI in Tandem Connection)
ODI (Outgoing Defect Indication)

H4:	x	x	1	1	x	x	LO Seq
-----	---	---	---	---	---	---	--------

LO Multiframe Sequence
xx11xx00: pointer to V1
xx11xx01: pointer to V2
xx11xx10: pointer to V3
xx11xx11: pointer to V4

H4:	MF12 (frames 0 and 1) SQ (frames 14 and 15)	Multiframe Indicator 1
-----	--	------------------------

VC-3/4-Xv sequence
bit 5-8: MF11 multiframe indicator (0 to 15)
frame 0 bit 1-4 MF12 MSB Multiframe Indicator 2
frame 1 bit 1-4 MF12 LSB
frame 14 bit 1-4 SQ MSB sequence indicator
frame 15 bit 1-4 SQ LSB sequence indicator

V5:	BIP-2	REI	RFI	Signal Label	RDI
-----	-------	-----	-----	--------------	-----

BIP-2 bit 1: Odd bit parity of the previous VC
bit 2: Even bit parity
REI (Receive Error Indication)
RFI (Remote Failure Indication)
VC signal label (mapping)
000 - Unequipped
001 - Reserved
010 - Asynchronous floating
011 - Bit synchronous
100 - Byte synchronous
101 - Extended signal label
110 - Test Signal 0.181
111 - VC-AIS
RDI (Remote Defect Indication)

K4:	ESL	VC	APS	E-RDI	DL
Z7:					

ESL (Extended Signal Label) 32 bits multiframe
bits 1-11 Multiframe Alignment
bits 12-19:
09: ATM
0A: HDLC/PPP
0B: HDLC/LAPS
0C: Concatenated test signal
bits 20-32: 0 (reserved for future)
VC (Lower Order Virtual Concatenation)
APS: Automatic Protection Switching channel
E-RDI (Enhanced RDI information)
(RDI=0) 010: Payload defect (PLM)
(RDI=1) 101: Server defect (AIS, LOP),
(RDI=1) 110: Connectivity defect (TIM, UNEQ)
DL: Lower Order Data Link

Figure 1.25 Nine-byte path overhead is attached to VC3, VC4, and VC4-Xc. Four-byte path overhead is attached to VC11, VC12, and VC2.

1.8.1 Path Overhead

The POH provides a communication protocol between the two ends of a VC path. Among these protocols are path performance monitoring, error and alarm indications, path protection, signals for maintenance purposes, and multiplex structure indications. There are two categories of virtual container POH (see Figure 1.25):

Table 1.5
Four-byte path overhead for VC-11, VC-12, VC-2, VC-2-Xc, VT-11, VT-12, and VT-6.

Byte	Description
V5	<i>LP general overhead</i> : Its position is indicated by the TU- <i>n</i> pointer, and it provides path status, performance monitoring, and signal label functions for VC-2, VC-12, and VC-11 paths. This byte enables continuous monitoring of anomalies and defects, and payload composition either at path end or at any point along the trail.
V5 _(bit1-2)	<i>LP bit error monitoring</i> : A BIP-2 is calculated by the transmitter over all the bits of the previous VC- <i>n</i> . The calculation includes POH bytes, but excludes V1, V2, V3 (except when used for negative justification), and V4.
V5 _(bit3)	<i>LP remote error indication (LP-REI)</i> : This is set to 1 and sent back toward an LP originator, if one or more bit errors is detected by the BIP-2.
V5 _(bit4)	<i>LP remote failure indication (LP-RFI)</i> , only VC-11: This is set to 1 and sent back if a failure is declared. Otherwise it is cleared (i.e., set to 0).
V5 _(bit5-7)	<i>LP signal label</i> : This indicates the payload composition. 0x: Unequipped, 1x: Reserved, 2x: Asynchronous, 3x: Bit-synchronous, 4x: Byte-synchronous, 5x: Extended signal label, see K4 bit 1, 6x: Test signal, O.181, 7x: VC-AIS.
V5 _(bit8)	<i>LP remote defect indication (LP-RDI)</i> : This is set to 1 and sent back towards the trail termination source if a failure condition is detected.
J2	<i>LP trace</i> : It carries on a configurable 16 sequence identifier (including a CRC-7 byte) so that the receiving path terminal could continuously verify its connection with the transmitter.
N2	<i>LP tandem connection monitoring function (LP-TCM)</i> : Bits 1-2: BIP-2 for TC bit error checking; bit 3: fixed to 1, bit 4: incoming AIS indicator (I-AIS), bit 5: indicates errored blocks (TC-REI), bit 6: OEI to indicate errored blocks, bits 7-8: operate as a 76-multiframe string, including access point identifier (TC-APId), TC-RDI, and ODI.
K4 _(bit1)	<i>Extended signal label</i> (if V5 _(bit5-7) are 5x): This is a 32-bit multiframe string. Bits 12 to 19 contain the label. 09x: ATM mapping, 0Ax: HDLC/PPP mapping, 0Bx: HDLC/LAPS mapping, 0Cx: test signal O.181 mapping, 0Dx: flexible topology data link mapping.
K4 _(bit2)	<i>LP virtual concatenation</i> : A 32-bit multiframe string.
K4 _(bit3-4)	<i>LP automatic protection switching channel (APS)</i> .
K4 _(bit5-7)	<i>LP enhanced remote defect indication</i> : Provides enhanced RDI information. 1x: no defect, 2x: payload defect (LP-PLM; loss of cell delineation or LCD), 5x server defects (LP-AIS, TU-LP), 6x: connectivity defects (LP-TIM, LP-UNEQ).
K4 _(bit8)	LP data link.

1. *Nine-byte path overhead*, or STS POH in SONET: When this structure is attached to C-4 or TUG-3, it creates a VC-4. It can also be attached to C-3 or TUG-2, in which case it creates a VC-3 (see Figure 1.25).
2. *Four-byte path overhead*, or VT POH in SONET: This structure is added to C-2, C-12, and C-11 to form a VC-2, VC-12, and VC-11 respectively. The four bytes are not just contiguous, but also part of a multiframe (see Figure 1.25).

The functionality of the nine-byte POH (see Table 1.4) and the four-byte POH (see Table 1.5) are very similar.

Table 1.6
Regenerator section overhead (RSOH) or section overhead (SOH).

<i>Byte</i>	<i>Description</i>
A1,	<i>Framing pattern</i> $A1=F6x$, $A2=28x$: Indicates the beginning of the STM frame. For STM- n , there are $3 \times n$ A1 bytes followed by $3 \times n$ A2 bytes.
A2	
J0	<i>Regenerator section trace</i> : This is used to transmit a 16- or 64-byte identifier (including a CRC-7 byte) repeatedly, so that every regenerator can verify its connection.
Z0	<i>Spare</i> : Reserved for future international standards.
B1	<i>RS bit error monitoring</i> : BIP-8 code using even parity, computed over all bits of the previous STM- n frame after scrambling. The value is placed into B1 before scrambling.
E1	<i>RS orderwire</i> : Provides a 64-kbit/s voice channel between regenerators.
F1	<i>User channel</i> : This can be used to provide data/voice channel for maintenance purposes.
D1-D3	<i>192-kbit/s data communication channel (DCC_R)</i> : between regenerators providing OAM functions.

1.8.2 Section Overhead

Section overhead (SOH) information is attached to the information payload to create an STM- n /OC- m frames (see Figure 1.26). This includes block framing information for maintenance, performance monitoring, and other operational functions. SOH information is classified into:

- *Regenerator section overhead* (RSOH): which is the interchange data unit between regenerator section layers (see Table 1.6).
- *Multiplex section overhead* (MSOH): which, passing transparently through regenerators, is the interchange data unit between multiplex section layers (see Table 1.7).

The SOH needs plenty of bytes to manage a wide range of functions. Among other things, it is responsible for the frame alignment, performance monitoring management channels, voice channels for communication between nodes, data channels used for synchronization, and protection services in case of physical layer failures.

Table 1.7
Multiplex section overhead (MSOH) or line overhead (LOH).

<i>Byte</i>	<i>Description</i>
B2	<i>MS bit error monitoring</i> : This is an IP- $n \times 24$ code is calculated over all bits of the previous STM- n frame, except for the three rows of SOH, and it is placed into the B2 bytes of the current frame.
K1, K2	<i>APS bytes</i> : They carry on the APS protocol (see Chapter 7).
K2 (bit6-8)	<i>MS-RDI</i> : This is used to return an indication (110) to the transmitting end that a defect has been detected or that MS-AIS (111) is received.
D4, D12	<i>MS data communication channel (DCC_M)</i> : This is a 576-kbit/s channel intended for OAM information for central management of multiplexer functions. The STM-256 frame has an additional 9,216-kbit/s channel which is carried in bytes from D13 to D156.
S1 (bit5-8)	<i>Synchronization status messages</i> : This is used to inform the remote multiplexer on the quality of the clock used to generate the signals. 0x: Unknown, 2x: G.811, 4x: G.812 transit, 8x: G.812 local, Bx: G.813, Fx: Not used for synchronization.
M1	<i>MS-REI</i> : The M1 returns the number of the detected BIP-24 $\times n$ errors to the remote multiplexer.
M0	<i>MS-REI</i> : This byte is concatenated with M1 to indicate a number of BIP violations greater than 256, (only STM-64 and STM-256).
E2	<i>MS orderwire</i> : Provides a 64-kbit/s voice channel for express orderwire between multiplex section terminations.
P1, Q1	<i>Optional forward error correction</i> : Defined only for STM-16, STM-64, and STM-256.

1.8.3 The SDH/SONET Hierarchy

We have already seen the STM-1 frame, equivalent to STS-3 and OC-1 in SONET, made up of a 9×270 byte matrix and transmitted at 155 Mbit/s. The hierarchy defines higher-order frames whose bit rates are obtained by multiplying successively by four. For simplicity, each bit rate is usually referred to by its rounded-off value (see Table 1.9).

The STM- n structure frame ($n = 4, 16, 64, 256$) consists of two section overheads (RSOH and MSOH) plus an AUG- n (see Table 1.8). Four AUG- n are block-interleaved, to create a superior structure referred to as AUG- $4n$. For instance, four AUG-4s are needed to create an AUG-16 (see Figure 1.27).

Table 1.8
AUG- n composition.

<i>AUG-1</i>	<i>AUG-4</i>	<i>AUG-16</i>	<i>AUG-64</i>	<i>AUG-256</i>
AU-4	AU4-4c	AU4-16c	AU4-64c	AU4-256c
3 x AU-3	4 x AUG-1	4 x AUG-4	4 x AUG-16	4 x AUG-64

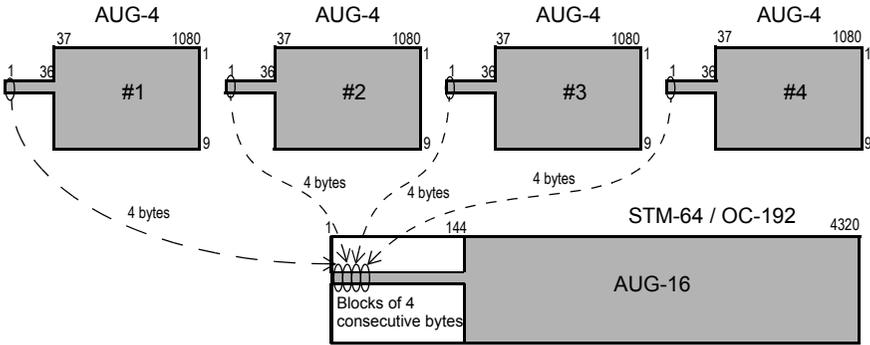


Figure 1.27 Multiplexing 4 AUG-*n* into an AUG-4*n* is block-interleaving, and the block size is exactly *n* bytes. 1, 4, and 16 are valid values for *n*.

Like the STM-1 frame, STM-*n* frames are represented as a rectangular structure of 270 x *n* columns and 9 rows, which gives a total of 270 x *n* x 9 = 2,430 x *n* bytes. Nonetheless, the frame period remains the same as that of the STM-1 frame: 125 μs. The new SOH is therefore 3 x 9*n* bytes, the multiplex section 3 x 9*n* bytes, and 9*n* bytes for AU-*n* pointers.

Table 1.9
Signals and information combinations.

<i>SDH</i>	<i>SONET Frame</i>	<i>SONET Optical</i>	<i>Size (Bytes)</i>	<i>Rate (Mbit/s)</i>	<i>Acronym</i>	<i>Capacity Samples</i>
STM-0	STS-1	OC-1	9x90	51.840	52M	28DS-1, DS-3, E3, 21E1
STM-1	STS-3	OC-3	9x270	155.520	155M	84DS-1, 3DS-3, E4, 3E3, 2E3+21E2, E3+42E2, 63E2
STM-4	STS-12	OC-12	9x1080	622.080	622M	4OC-3, 4 STM-1
STM-16	STS-48	OC-48	9x4320	2488.320	2.5G	16OC-3, 16 STM-1
STM-64	STS-192	OC-192	9x17280	9953.280	10G	64OC-3, 64 STM-1
STM-256	STS-768	OC-768	9x69120	39814.120	40G	256OC-3, 256 STM-1

When looking at the STM-*n*/OC-*m* frames, the concept of indirect multiplexing cannot be ignored. To explain this, let us look at the example of the STM-16 frame. Forming one of these frames by direct multiplexing means that it has been formed by interleaving bytes from 16 STM-1 frames. An STM-16 structure can also be obtained from four STM-4 frames, by indirect multiplexing. In this case, interleaving is carried out in blocks of 4 bytes. The resulting structure is therefore the same for both cases.

In addition to its functions outlined in previous sections, the pointer mechanism also facilitates the construction of STM-*n*. In effect, due to the imperfection that is inherent to synchronization, STM frames reach multiplexers with random relative alignments; that is, some of them are out of phase in respect to others. Nonetheless, the STM-*n* higher-order frame that leaves the multiplexer keeps its bytes grouped together in a single block. The payloads of the frames can be interleaved without prior alignment, since virtual containers will have a pointer value that has been recalculated in the overhead of the outgoing frame.

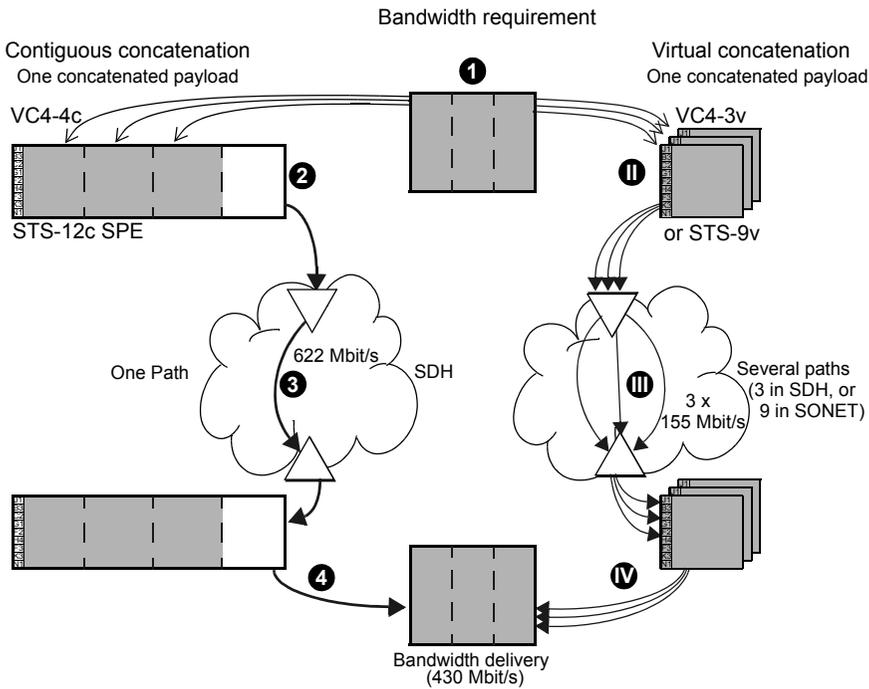


Figure 1.28 An example of contiguous concatenation and virtual concatenation. Contiguous concatenation requires support by all the nodes. Virtual concatenation allocates bandwidth more efficiently, and can be supported by legacy installations.

1.9 CONCATENATION

Concatenation is the process of summing the bandwidth of *X* containers (*C-i*) into a larger container. This provides a bandwidth *X* times bigger than *C-i*. It is well indicated for the transport of big payloads requiring a container greater than VC-4, but it is also possible to concatenate low-capacity containers, such as VC-11, VC-12, or VC-2.

There are two concatenation methods (see Figure 1.28):

1. *Contiguous concatenation*: which creates big containers that cannot split into smaller pieces during transmission. For this, each NE must have a concatenation functionality.
2. *Virtual concatenation*: which transports the individual VCs and aggregates them at the end point of the transmission path. For this, concatenation functionality is only needed at the path termination equipment.

1.10 MAINTENANCE

SDH and SONET transmission systems are robust and reliable; however they are vulnerable to several effects that may cause malfunction. These effects can be classified as follows:

- *Natural causes*: This include thermal noise, always present in regeneration systems; solar radiation; humidity and Raleigh fading² in radio systems; hardware aging; degraded lasers; degradation of electric connections; and electrostatic discharge.
- *A network design pitfall*: Bit errors due to bad synchronization in SDH. Timing loops may collapse a transmission network partially, or even completely.
- *Human intervention*: This includes fiber cuts, electrostatic discharges, power failure, and topology modifications.

All these may produce changes in performance, and eventually collapse transmission services.

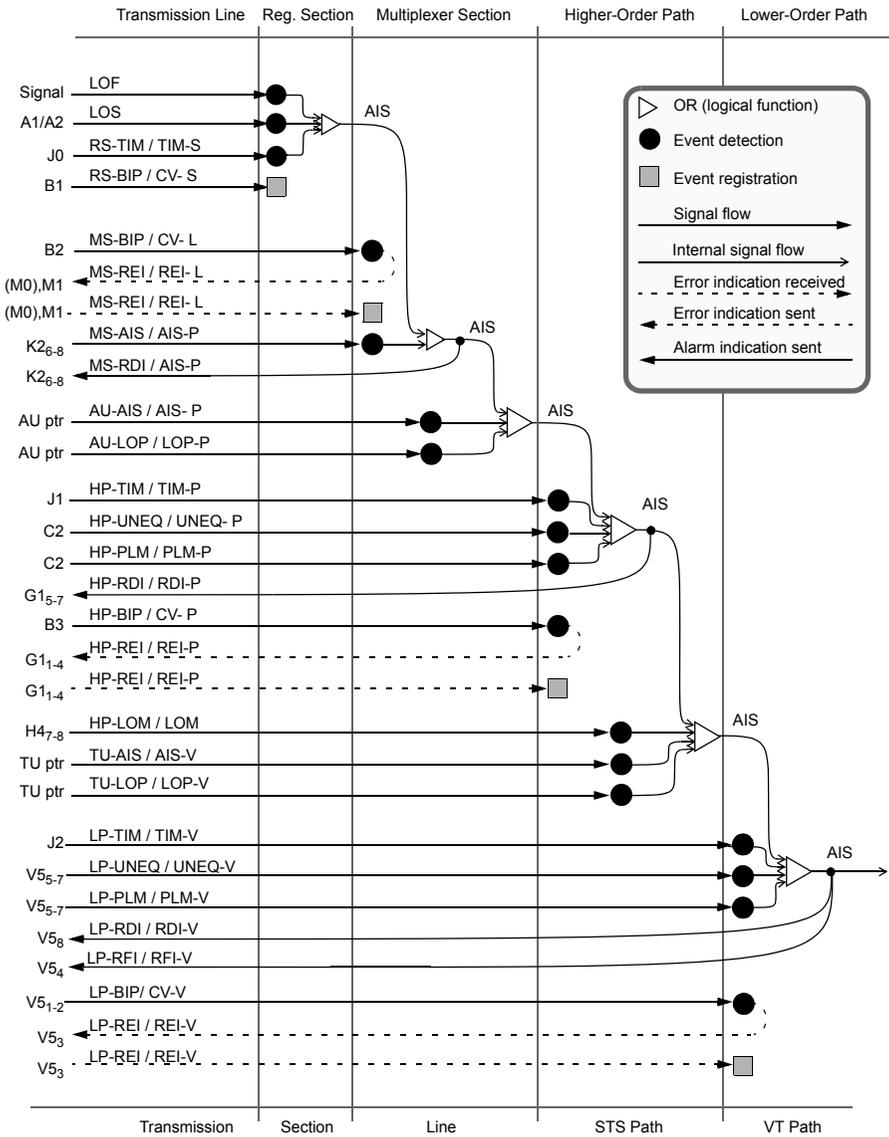
1.10.1 SDH/SONET Events

SDH/SONET events are classified as anomalies, defects, damage, failures, and alarms depending on how they affect the service:

- *Anomaly*: This is the smallest disagreement that can be observed between measured and expected characteristics. It could for instance be a bit error. If a single anomaly occurs, the service will not be interrupted. Anomalies are used to monitor performance and detect defects (see Section 1.11).

2. Raleigh fading is the phenomenon in which the field detected at the receiver is the sum of many random contributions of different phases and directions, due to multipath effects.

SDH



SONET

Figure 1.29 Anomalies and defects management. (In regular characters for SDH; in italic for SONET.)

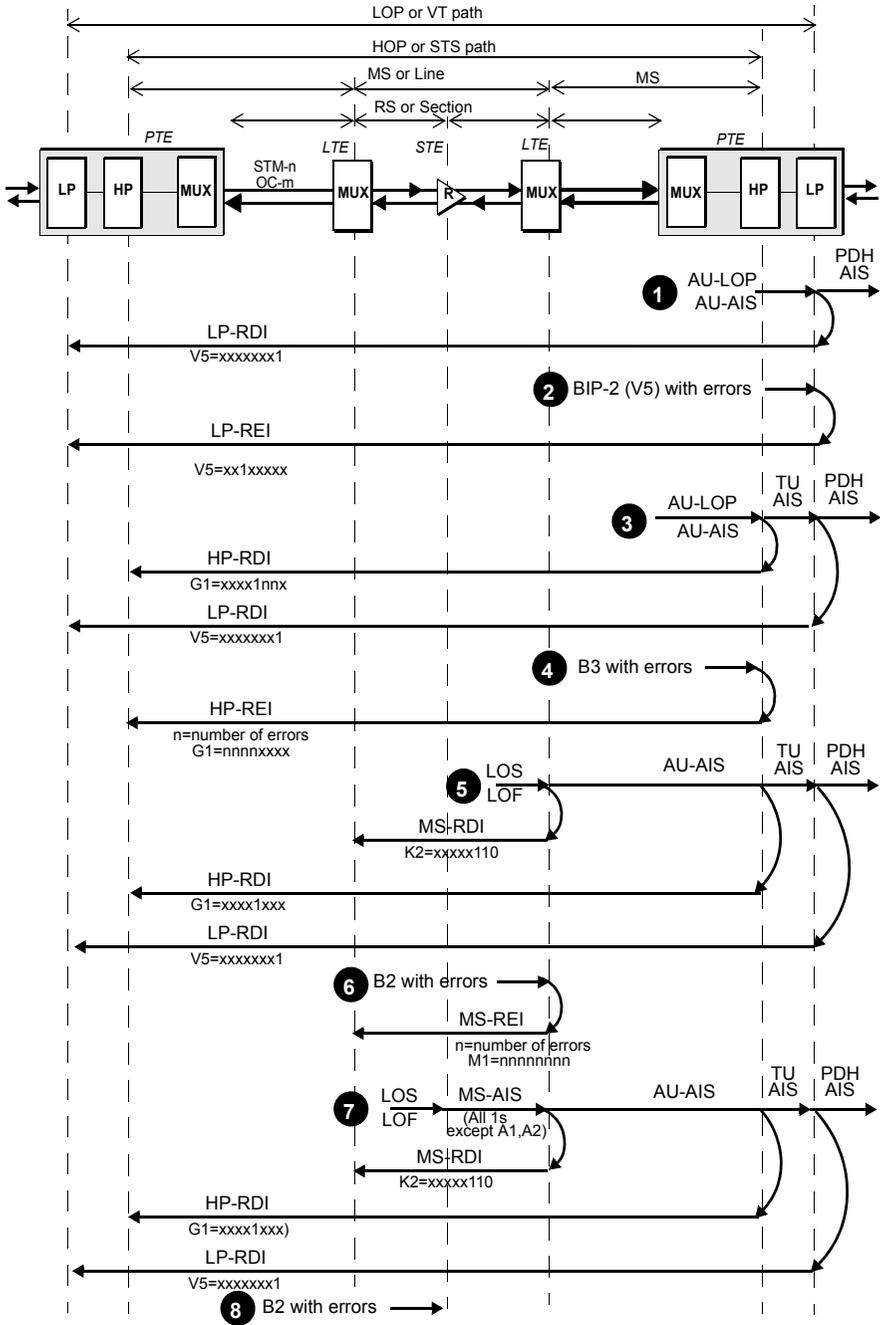


Figure 1.30 OAM management. Signals are sent downstream and upstream when events are detected at the LP edge (1, 2); HP edge (3, 4); MS edge (5, 6); and RS edge (7, 8).

- *Defect*: A defect level is reached when the density of anomalies is high enough to interrupt a function. Defects are used as input for performance monitoring, to control consequent actions, and to determine fault causes.
- *Damage or fault*: This is produced when a function cannot finish a requested action. This situation does not comprise incapacities caused by preventive maintenance.
- *Failure*: Here, the fault cause has persisted long enough so that the ability of an item to perform a required function may be terminated. Protection mechanisms can now be activated (see Section 1.13).
- *Alarm*: This is a human-observable indication that draws attention to a failure (detected fault), usually giving an indication of the depth of the damage. For example, a *light emitting diode* (LED), a siren, or an e-mail.
- *Indication*: Here events are notified upstream to the peer layer for performance monitoring and eventually to request an action or a human intervention that can fix the situation (see Figure 1.29).

Errors reflect anomalies, and alarms show defects. Terminology here is often used in a confusing way, in the sense that people may talk about errors but actually refer to anomalies, or use the word, “alarm” to refer to a defect.

In order to support a single-end operation the defect status and the number of detected bit errors are sent back to the far-end termination by means of indications such as RDI, REI, or RFI (see Figures 2.31 and 2.32).

1.10.2 Monitoring Events

SDH frames contain a lot of overhead information to monitor and manage events (see Table 1.16). When events are detected, overhead channels are used to notify peer layers to run network protection procedures or evaluate performance. Messages are also sent to higher layers to indicate the local detection of a service affecting fault to the far-end terminations.

Defects trigger a sequence of upstream messages using G1 and V2 bytes. Downstream AIS signals are sent to indicate service unavailability. When defects are detected, upstream indications are sent to register and troubleshoot causes.

1.10.3 Event Tables

Tables 2.12-2.16 summarize events and indications associated with each SDH layer. Testing events have also been included.

Table 1.10
Regenerator and multiplex section events and indications.

<i>SDH</i>	<i>SONET</i>	<i>Type</i>	<i>How</i>	<i>Comments</i>
LOS	LOS	Defect	BER>limit	Loss of signal detection
ECOD	ECOD	Anomaly	Code error	Line code violation
OOF	OOF	Anomaly	A1-A2	Out of frame detection
LOF	LOF	Defect	A1-A2	Loss of frame detection
RS-TIM	TIM-S	Defect	J0	Trace identifier mismatch
B1 error	B1 error	Anomaly	B1	Bit error detected by BIP-8 verification
B2 error	B2 error	Anomaly	B2	Bit error detected by BIP-24 verification
MS-REI	REI-L	Indication	M1=xxx M0= xxx	Number of errors detected using B2 M0 is used by STM-64 and STM-256 only
MS-AIS	AIS-L	Alarm	K2 ₍₆₋₈₎ =111	Mux/line alarm indication signal detection
MS-RDI	RDI-L	Indication	K2 ₍₆₋₈₎ =110	Mux/line remote defect indication

Table 1.11
Path events and indications.

<i>SDH</i>	<i>SONET</i>	<i>Type</i>	<i>How</i>	<i>Comments</i>
HP-TIM	TIM-P	Defect	J1	Trace identifier mismatch in path
B3 error	B3 error	Anomaly	B3	Bit error detected by BIP-24 verification
HP-REI	REI-P	Indication	G1 ₍₁₋₄₎ =xxxx	Number of errors detected using B3
HP-UNEQ	UNEQ-P	Defect	C2 ₍₁₋₈₎ =0	Unequipped or supervisory unequipped
HP-PLM	PLM-P	Defect	C2 ₍₁₋₈₎ =x	Payload label mismatch
HP-RDI	RDI-P	Indication	G1 ₍₅₋₇₎ =010	Payload defect PLM
HP-RDI	RDI-P	Indication	G1 ₍₅₋₇₎ =101	Server defect. AIS or loss of pointer (LOP)
HP-RDI	RDI-P	Indication	G1 ₍₅₋₇₎ =110	Connectivity defect. TIM or UNEQ
HP-LOM	LOM-V	Defect	H4	Loss of multiframe (H4 is in POH)
LP-TIM	TIM-V	Defect	J2	Trace identifier mismatch in path
BIP-2 error	BIP-2 error	Anomaly	V5 ₍₁₋₂₎	Error detected by BIP-2 verification
LP-REI	REI-V	Indication	V5 ₍₃₎ =1	One or more errors detected by BIP-2 in V5
LP-RFI	RFI-V	Indication	V5 ₍₄₎ =1	Remote failure indication lower-order path
LP-UNEQ	UNEQ-V	Defect	V5 ₍₅₋₇₎ =0	Unequipped or supervisory unequipped
LP-PLM	PLM-V	Defect	V5 ₍₅₋₇₎ =x	Payload label mismatch
LP-RDI	RDI-V	Indication	V5 ₍₈₎ =1	Remote defect indication lower-order path

Table 1.12
Pointer events.

<i>SDH</i>	<i>SONET</i>	<i>Type</i>	<i>How</i>	<i>Comments</i>
AU-NDF	NDF-P	Ptr event	H1, H2	New AU Pointer (STS pointer in SONET)
AU-PJE	PJE-P	Ptr event	H1, H2	Pointer justification
AU-Inv	Inv-P	Ptr event	H1, H2	Pointer inversion
AU-Inc	Inc-P	Ptr event	H1, H2	Pointer increment
AU-Dec	Dec-P	Ptr event	H1, H2	Pointer decrement
AU-LOP	LOP-P	Defect	H1, H2	Loss of pointer
AU-AIS	AIS-P	Alarm	H1, H2	Alarm indication signal detection
TU-NDF	NDF-V	Ptr event	V1, V2	New TU pointer
TU-PJE	PJE-V	Ptr event	V1, V2	Pointer justification
TU-Inv	Inv-V	Ptr event	V1, V2	Pointer inversion
TU-Inc	Inc-V	Ptr event	V1, V2	Pointer increment
TU-Dec	Dec-V	Ptr event	V1, V2	Pointer decrement
TU-LOP	LOP-V	Defect	V1, V2	Loss of pointer
TU-AIS	AIS-V	Alarm	V1, V2	Alarm indication signal detection

Table 1.13
Tandem connection monitoring events.

<i>SDH/SONET</i>	<i>Type</i>	<i>How</i>	<i>Comments</i>
HPTC-LTC LPTC-LTC	Defect	N1 ₍₇₋₈₎ (frames 1-8) N2 ₍₇₋₈₎ (frames 1-8)	Higher/lower-order path tandem connection loss of tandem connection monitoring.
HPTC-TIM LPTC-TIM	Defect	N1 ₍₇₋₈₎ (frames 9-72) N2 ₍₇₋₈₎ (frames 9-72)	Higher/lower-order path tandem connection trace identifier mismatch.
HPTC- UNEQ LPTC-UNEQ	Defect	N1=0 N2=0	Higher/lower-order path tandem connection unequipped
HPTC-RDI LPTC-RDI	Indication	N1 ₍₈₎ (frame 73) N2 ₍₈₎ (frame 73)	Higher/lower-order path tandem connection remote defect indication
HPTC-AIS LPTC-AIS	Indication	N1 ₍₁₋₄₎ =1110 N2 ₍₄₎ =1	Higher/lower-order path tandem connection alarms indication signal
HPTC-IEC LPTC-IEC	Anomaly	N1 ₍₁₋₄₎ =xxxx N2 ₍₁₋₂₎ =xx	Higher/lower-order path tandem connection incoming error count
HPTC-ODI LPTC-ODI	Indication	N1 ₍₇₎ (frame 74) N2 ₍₇₎ (frame 74)	Higher/lower-order path tandem connection outgoing defect indication
HPTC-REI LPTC-REI	Indication	N1 ₍₅₎ =1 N2 ₍₅₎ =1	Higher/lower-order path tandem connection remote error indication
HPTC-OEI LPTC-OEI	Indication	N1 ₍₆₎ =1 N2 ₍₆₎ =1	Higher/lower-order path tandem connection outgoing error indication

Table 1.14

Line and test sequence events. These events do not depend on the digital hierarchy, but are only related to the test sequences used, or to the characteristics of the signal.

<i>SDH</i>	<i>SONET</i>	<i>Type</i>	<i>Detection</i>	<i>Cause</i>
TSE	TSE	Anomaly	Test pattern	Test sequence error (O.181)
LSS	LSS	Anomaly	Test pattern	Loss of sequence synchronization
Slip	Slip	Fault	Test pattern	PLL buffer overflow or underflow
LTI	LTI	Fault	Test equipment	Loss of timing input
Optical saturation		Fault	Optical receiver	Optical power mismatch

1.11 PERFORMANCE MONITORING

SDH has performance monitoring capabilities based on bit error monitoring. A bit parity is calculated for all bits of the previous frame, and the result is sent as overhead. The far-end element repeats the calculation and compares it with the received overhead. If the result is equal, there is considered to be no bit error; otherwise, a bit error indication is sent to the peer end.

1.11.1 Bit Error Checking

Bit error monitoring is based on checking the value of certain groups of bits that make up *bit interleaved parity* (BIP) words as a checksum. This way, there is parity checking between regenerators, multiplex sections, and paths (see Figure 1.31). If the received signal contains bit errors, a BIP indication is generated that is treated as an anomaly, and an REI indication is sent to the far end (see Table 1.15).

Table 1.15
Bit interleaved parity bytes

<i>Byte</i>	<i>BIP</i>	<i>SDH</i>	<i>BIP area</i>	<i>REI</i>
B1	BIP-8	Reg section	STM/STS frame	—
B2	BIP-8/BIP-24	Multiplex section	Frame excluding RSOH	MS-REI
B3	BIP-8	Higher-order path	HO virtual container	LO-REI
V5 ₍₁₋₂₎	BIP-2	Lower-order path	LO virtual container	HO-REI

Network elements themselves make certain decisions after evaluating the frame received and generating a new one to the next NE. BIP is a continuous monitoring process that provides the operator with a powerful error detection tool, and activates the corresponding mechanisms to deal with detected anomalies and also to permit evaluation of the performance of the network (see Chapter 7).

1.11.2 Tandem Connection Monitoring

Tandem connection monitoring (TCM) is a sublayer between the multiplex section and path layers. A tandem connection transports the virtual container in a reliable way when it is routed via networks of different operators. When a bit error occurs, the TCM protocol informs the network about its location (see Figure 1.32).

This mechanism calculates the number of bit errors that occurs when the VC enters the subnetwork. When the VC arrives at the subnetwork end, the number of bit errors is computed again, and the two results are compared. The input point is called the *TCM source* and the output point the *TCM sink*:

1. The number of bit errors detected (by means of the BIP-8) in the incoming VC-*n* at the TCM source is written to the *incoming error count* (IEC) (see Table 1.13).
2. When the VC-*n* arrives at the TCM sink, the number of bit errors is calculated again, and, if the figure is different from the IEC, this tells us that new bit errors have occurred.

1.11.3 Forward Error Correction

Forward error correction (FEC) can reduce *bit error rate* (BER) in optical transmission, providing correction capabilities at the receiving end. The mathematical algorithm used to implement FEC in SDH is *Bose-Chaudhuri-Hocquenghem*

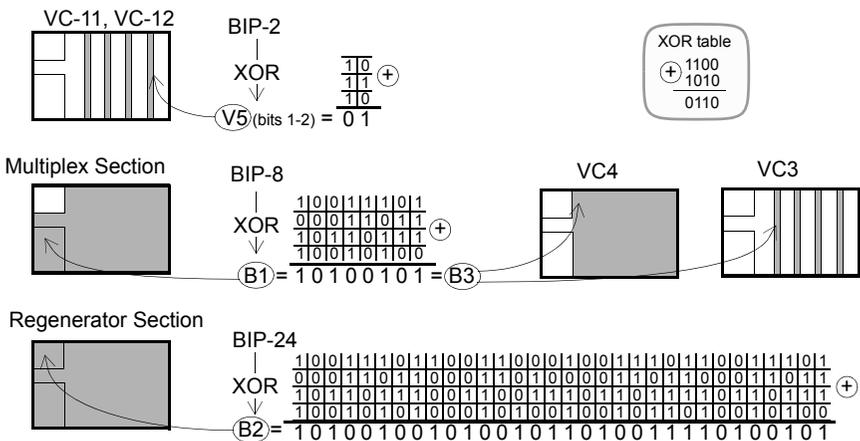


Figure 1.31 Bit interleaved parity (BIP-*n*) enables error monitoring. A transmitter performs the *exclusive or* (XOR) function (even parity) over the previous block. The value computed is placed in the *n* bits before the block is scrambled.

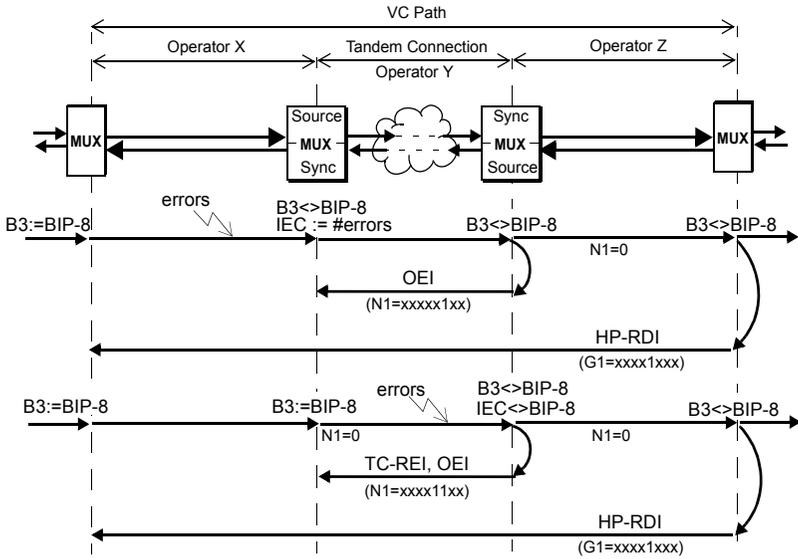


Figure 1.32 Tandem connection monitoring sample: Three operators transporting a higher-order payload.

(BCH). BCH is performed in the data being transported, and the results are stored in the P1 and Q1 bytes of the RS and MS sections. At the receiving end, we check if bit errors have occurred, and, if so, we correct them. FEC is defined for STM-16, STM-64, and STM-256, and it uses MSOH and RSOH overhead bytes, providing correction for the AUG-n area.

1.12 DEFECTS

A defect is understood as any serious or persistent event that holds up the transmission service. SDH defect processing reports and locates failures in either the complete end-to-end circuit (HP-RDI, LP-RDI) or on a specific multiplex section between adjacent SDH nodes (MS-RDI) (see Figure 1.29).

Alarm indication signal

An alarm indication signal (AIS) is activated under standardized criteria (see Table 1.16), and sent downstream in a path in the client layer to the next NE to inform about the event (see Figure 1.29). The AIS will arrive finally at the NE at which that path terminates, where the client layer interfaces with the SDH network (see Figure 1.30).

Table 1.16
Analysis criteria of SDH/SONET events.

<i>Event</i>	<i>Criterion</i>
LOS	<i>Loss of signal:</i> This parameter should be raised when incoming power at the receiver has dropped to a level that produces a high BER. LOS indicates either a transmitter failure or an optical path break. Timing requirements for detection and reset fall within regional standards.
OOF	<i>Out of frame:</i> This is raised when five frames are received with error in the FAS (incorrect patterns in A1 and A2). The maximum OOF detection is 625 μ s and it should be cleared after receiving one correct frame (ITU-T G.783, ANSI T1.231).
LOF	<i>Loss of frame:</i> OOF events are collectively referred to as LOF. If the OOF state persists for 2.5 ms \pm 0.5 ms, an LOF should be declared. LOF should be left after 2.5 ms without OOF (ITU-T G.783, ANSI T1.231).
LOP	<i>Loss of pointer:</i> The LOP state is entered in the case of n consecutive invalid pointers ($8 \leq n \leq 10$) or n consecutive new data flag (NDF) enable flags ($8 \leq n \leq 10$). The LOP state should be cleared after three consecutive valid pointers or three consecutive AIS indications (G.783, ANSI T1.231). In SDH: AU-LOP, TU-LOP. In SONET: LOP-P, LOP-V.
LOM	<i>Loss of multiframe:</i> H4 byte does not track the multiframe sequence during eight frames. (ITU-T G.783). In SDH: HP-LOM. In SONET: LOM.
UNEQ	<i>Unequipped connectivity defect:</i> C2 or V5 is equal to "0" during five consecutive frames (ITU-T G.783, ANSI T1.231). In SDH: HP-UNEQ, LP-UNEQ. In SONET: UNEQ-P, UNEQ-V.
TIM	<i>Trace identifier mismatch connectivity defect:</i> The CRC of the J1 or J2 identifier does not match during n consecutive frames (ITU-T G.783, ANSI T1.231). In SDH: HP-TIM, LP-TIM. In SONET: TIM-P, TIM-V.
PLM	<i>Payload label mismatch payload defect:</i> The C2 or V5 contents are not consistent with the specified label during five consecutive frames (ITU-T G.783, ANSI T1.231). In SDH: HP-PLM, LP-PLM. In SONET: PLM-P, PLM-V.
REI	<i>Remote error indication:</i> This indication contains the number of bit errors detected at the receiving node. REI is sent back to the far end to allow bit error monitoring and single-end control (ITU-T G.707, ANSI T1.231). In SDH: MS-REI, HP-REI, LP-REI, TC-REI. In SONET: REI-L, REI-P, REI-V, TC-REI.

Table 1.16
Analysis criteria of SDH/SONET events.

RDI	<p><i>Remote defect indication:</i> This indication is sent to the transmission end upon detecting LOS, LOF, or AIS defect. This indication was known previously as FERF. RDI should be detected before five consecutive frames with G1 or V5 arisen. (ITU-T G.783, ANSI T1.231).</p> <p>In SDH: MS-REI, HP-RDI, LP-RDI, TC-REI. In SONET: RDI-L, RDI-P, REI-V, TC-REI.</p>
AIS	<p><i>Alarm indication signal:</i> This indication is an all-ones signal. It is generated to replace the normal traffic signal when it contains a defect. The receiver has to detect it after three consecutive frames with K2=xxxxx111 or H1, H2 = 11111111 (ITU-T G.783, ANSI T1.231).</p> <p>In SDH: MS-AIS or SONET: AIS-L. In SDH: AU-AIS, TU-AIS or SONET: AIS-P, AIS-L.</p>
RFI	<p><i>Remote failure indication:</i> This indication is sent when a defect persists for a period of time. RFI is returned to the transmission end when a LOS, LOF, or AIS surpasses a predetermined period of time to activate the protection switch protocol to provide an alternative path.</p> <p>In SDH: LP-RFI. In SONET: RFI-L, RFI-P, RFI-V.</p>
LSS	<p><i>Loss of sequence synchronization:</i> This signal is activated during a test when a pseudo-random pattern is generated in one extreme, and on the receiver side the BER > 0.20 during 1 second; or long duration AIS; or uncontrolled bit slip; or loss of signal (M.2100).</p>

As an answer to a received AIS, a remote defect indication is sent backwards. An RDI is indicated in a specific byte, while an AIS is a sequence of “1s” in the payload space. The permanent sequence of “1s” tells the receiver that a defect affects the service, and no information can be provided.



Figure 1.33 AIS formats.

Depending on which service is affected, the AIS signal adopts several forms (see Figure 1.33):

- *MS-AIS:* All bits except for the RSOH are set to the binary value “1.”

- *AU-AIS*: All bits of the administrative unit are set to “1” but the RSOH and MSOH maintain their codification.
- *TU-AIS*: All bits in the tributary unit are set to “1,” but the unaffected tributaries and the RSOH and MSOH maintain their codification.
- *PDH-AIS*: All the bits in the tributary are “1.”

Enhanced remote defect indication

Enhanced remote defect indication (E-RDI) provides the SDH network with additional information about the defect cause by means of differentiating:

- *Server defects*: like AIS and LOP;
- *Connectivity defects*: like TIM and UNEQ;
- *Payload defects*: like PLM.

Enhanced RDI information is codified in G1 (bits 5-7) or in k4 (bits 5-7), depending on the path.

1.13 SDH RESILIENCE

Security consists of a series of contingency procedures to recover the voice/data service through a new path when the previous becomes unavailable because a network resource, such as a link or a node, fails. Fault detection, excessive bit error rate, AIS detection or a network management request are common reasons for security procedures to run. Security strategies in transmission networks can be grouped as follows:

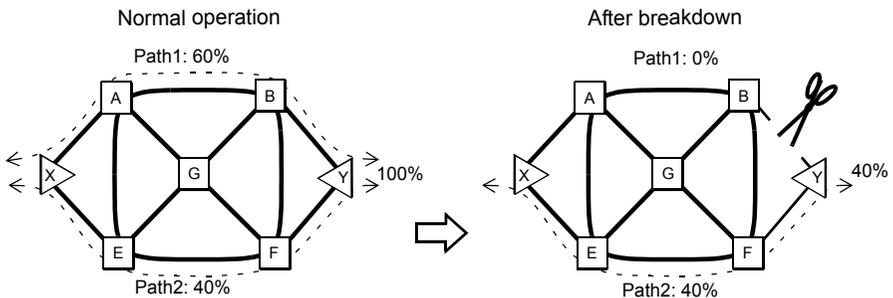


Figure 1.34 Diversification strategy between points X and Y.

Diversity

This strategy consists of dividing paths between two points into different routes (see Figure 1.34). A breakdown on one of the routes will affect only a portion of the total traffic. This method, which has largely been applied to legacy networks, can also be applied to SDH by using virtual concatenation and sending the traffic through several paths. Service is restored only when the resource is repaired.

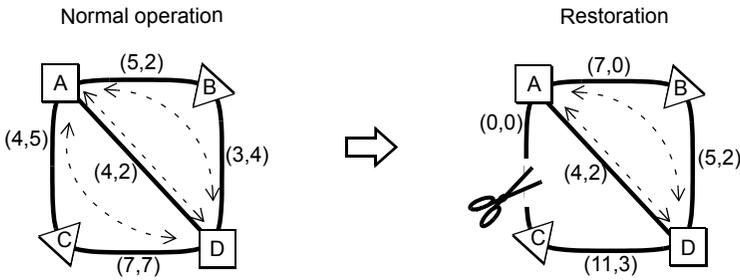


Figure 1.35 Restoration sample, whereby every connection is defined by a couple (x, y), where “x” is the number of active circuits, and “y” is the number of protection circuits.

Restoration

This scheme calls for special nodes and external control software permanently analyzing service failures (see Figure 1.35). When the process is triggered, an alternative route is selected from spare resources that are used on demand instead of being preassigned. Everything can be replaced, including terminal nodes. Recovery time is within the range of several minutes.

Protection

This mechanism preassigns spare resources when the working ones are faced with failure. This type of recovery is controlled from the network elements themselves, using internal information rather than control software like in restoration. Recovery time is within the range of milliseconds.

1.13.1 Protection Basics

There is set of strategies that can be called *protection*. All of them use internal information of the SDH network to configure fault-tolerant networks. In the following, we shall briefly look at some protection-related concepts:

- *Working or protection resources:* Working resources (lines, nodes, paths, sections) transport traffic during normal operation. Protection resources are there to replace them after a network failure (see Figure 1.37).
- *Active and passive protection:* Active protection uses a protocol to specify the protection action, and recovery time depends on the number of nodes which need to be controlled to be below the limits. Passive protection is less sophisticated and independent of the number of nodes.
- *Automatic protection switching:* APS is the standard capacity of automatic recovery after a failure at the multiplex section layer. K1 and K2 bytes are used to manage the protection protocol (see Figures 2.38 and 2.39).
- *Dedicated protection and shared protection:* In dedicated protection each working channel has a protection channel. In shared protection n protection channels are used by m channels to be protected (see Figure 1.36). See also 1+1 or 1:n configurations.
- *1+1 or 1:n configurations:* 1+1 means dedicated protection, where the protected signal is sent to the destination on two separate channels. No special protocol is needed, since the best signal is selected at the reception end. The switch threshold is programmable; usually based on BIP error rate. This is a simple and fast configuration that performs a 100% restoration, but it is also expensive. 1:n configuration means shared protection, where the n number of working channels are protected by one protection channel using the APS protocol. The protection channel can transmit an idle signal or extra traffic. It is cheaper, but its downside is that it does not perform 100% restoration (see Figure 1.37).
- *Unidirectional or bidirectional protection:* In a normal situation, a unidirectional ring routes traffic only in one direction (i.e., clockwise). A bidirectional ring routes traffic in both directions. After a failure has occurred in one direc-

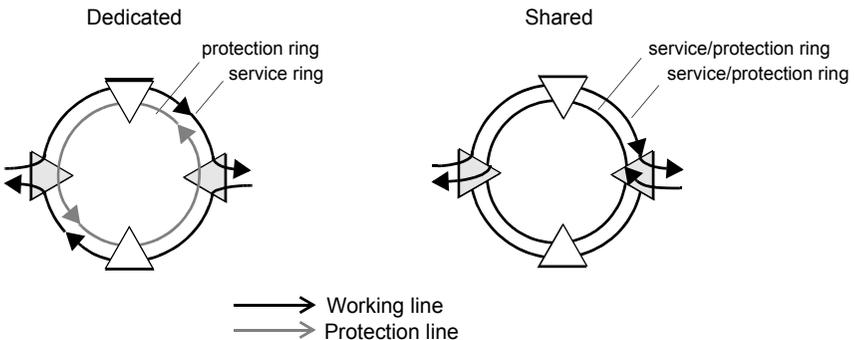


Figure 1.36 Shared and dedicated protection architectures.

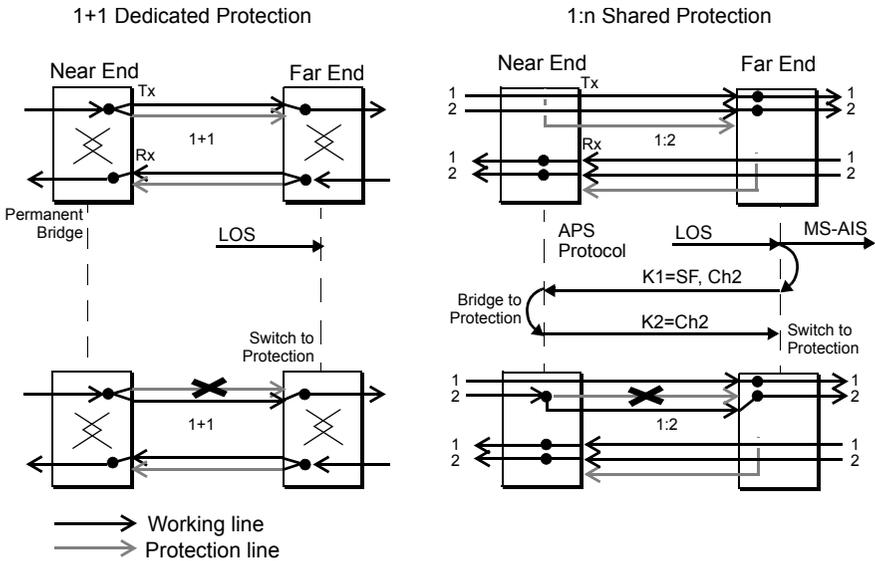


Figure 1.37 MSP protection. In 1+1 dedicated protection incoming signals are permanently bridged at far end. In 1:n shared protection working facilities use a common facility and APS protocol is required to manage the procedure. To be more effective, working and protection resources should take a different geographical path.

tion, a bidirectional strategy switches both directions, affected or unaffected. When it comes to the unidirectional strategy, only the affected direction is switched (see Figure 1.38).

- *Ring-switching or span-switching:* During a ring switch, the traffic is carried over the protection channels on the long path. During a span switch, the traffic is carried over the protection channels on the same span as the failure. Span switch is similar to 1:1 linear protection, but applies only to four fiber rings (see Figure 1.40).
- *Dual-ended or single-ended protection:* See unidirectional/bidirectional protection.
- *Trail or subnetwork protection:* Trail protection is used when the protected resource is a path or a multiplex section. If this is not the case, the scheme is classified as subnetwork protection; for instance, in the case of the route between two DXCs (see Figure 1.41).
- *Revertive or non-revertive protection:* If revertive protection is used, the normal data flow reverts to the original working resources once a failure has been repaired. This scheme is used in 1:n configuration. Protection is non-revertive if the protection channel, is treated as a working channel and the flow does not return to the original resources. This is used in 1+1 configurations.

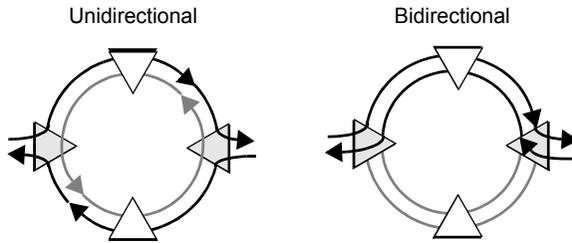


Figure 1.38 Unidirectional and bidirectional protection strategies.

- *Bridge/switch signals:* A bridged signal means that it is sent over two fibers. On the reception side the best signal is switched or selected.

Protection is a wide concept that can be implemented using a number of different strategies. Some of the most common are presented below. For more information, refer to ITU-T Rec. G.707 and G.841.

1.13.2 Multiplex Section or Line Protection

Multiplex section protection (MSP) schemes protect all the traffic flowing through a multiplex section without any discrimination. Switching actions are generally managed by the APS protocol using the K1 and K2 bytes. The protection switching actions must be initiated within 10 ms after detecting signal fails, and traffic must be restored within 50 ms. This means that transport service should be restored within 60 ms after the fault.

Multiplex section linear protection

In *multiplex section linear protection (MSLP)*, a working line is protected by a dedicated protection facility. The simplest implementation uses a 1+1 configuration, and traffic is transmitted simultaneously along working and protection lines, with the better of the two signals selected at the receiving end. 1:n configuration is also possible (see Figure 1.37). In that case “n” working lines share a unique protection line.

Multiplex section dedicated protection ring

A *multiplex section dedicated protection ring (MSDPRING)* is a unidirectional ring using a 1:1 dedicated protection scheme. The ring has two fibers: one working fiber and one protection fiber. Since traffic only travels in one direction unless a fail occurs, affected traffic is bridged at the entry node (see Figure 1.39).

Multiplex section shared protection

A *multiplex section shared protection* (MSSPRING) is a bidirectional ring using a 1:n shared protection scheme. The principle of sharing is based on the idea that working channels and protection channels share the same multiplex section. Any section can have access to the protection channels when a failure occurs. MSSPRING can be categorized into two types: two fiber and four fiber rings.

1. *Two fiber ring*: Each fiber carries both working and protection channels permanently. Working channels in one fiber are protected by the protection channels traveling in the opposite direction around the ring. Only ring switching is possible (see Figure 1.40).
2. *Four fiber ring*: Working and protection channels are carried over different fibers. Two multiplex sections transmitting in opposite directions carry the working channels, while two multiplex sections, also transmitting in opposite directions, carry the protection channels. This scheme allows both span switching and ring switching (see Figure 1.40).

Span switching is a simple scheme equivalent to 1:1 protection between two adjacent nodes. Ring switching is more complex, but prevents node faults and multiple fiber failures when routing the traffic away from the problem.

As in the previous case, the protection channels can transport low-priority traffic when they are not carrying out their protection function.

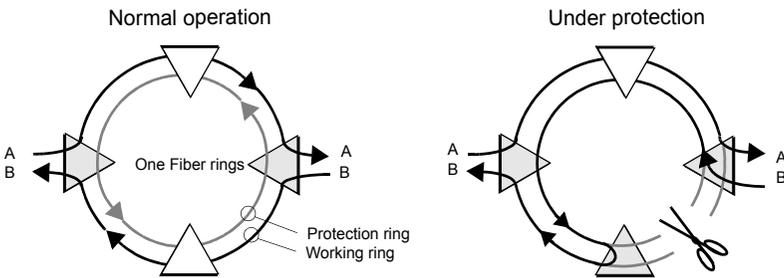


Figure 1.39 Multiplex section dedicated protection ring (MSDPRING) also known as *unidirectional self-healing ring* (USHR). The counterrotating ring provides the protection.

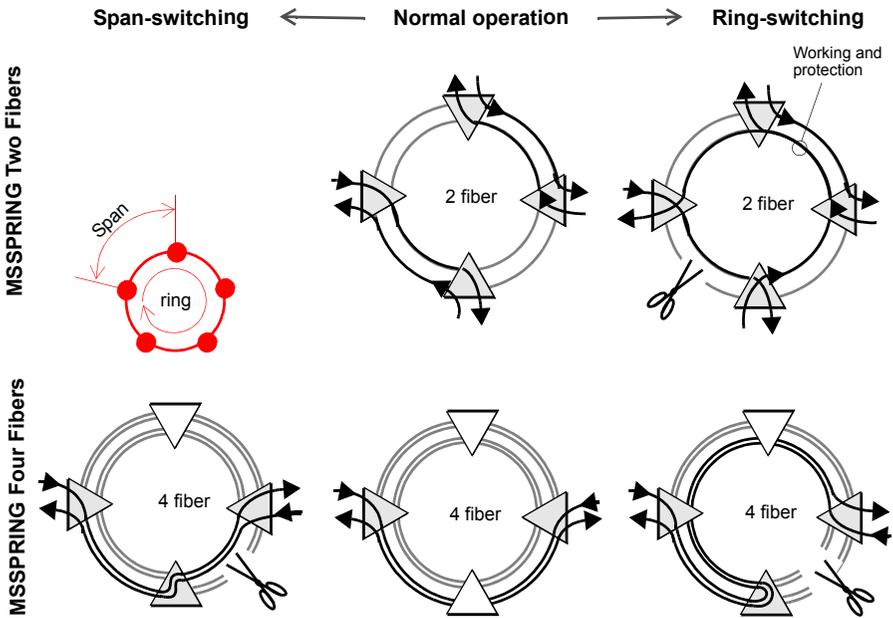


Figure 1.40 Multiplex section shared protection ring (MSSPRING) also known as bidirectional self healing ring (BSHR). Two fiber rings only allow for ring switching, while four fiber rings enable both span and ring switching.

1.13.2.1 VC path protection

Virtual container path protection (VC-P): This scheme allows the protection of individual virtual containers across the whole path where physically separated routes exist. The protection can be across different sections and different operators. The switching actions are managed at a higher level using the K3 (to protect VC3, VC4) or K4 (to protect VC11, VC12, VC2).

VC-P is a dedicated end-to-end protection that can be used in meshed, linear, and rings topologies. The protection switching may be either unidirectional or bidirectional (see Figure 1.41).

1.13.2.2 Subnetwork connection protection

Subnetwork connection protection (SNC-P), equivalent to SONET unidirectional path switched rings, is a 1+1 linear protection scheme. If VC-P provides surveillance to the whole path, SNC-P offers protection between two points on a path. The protection can switch on server failures using either inherent monitoring, such as

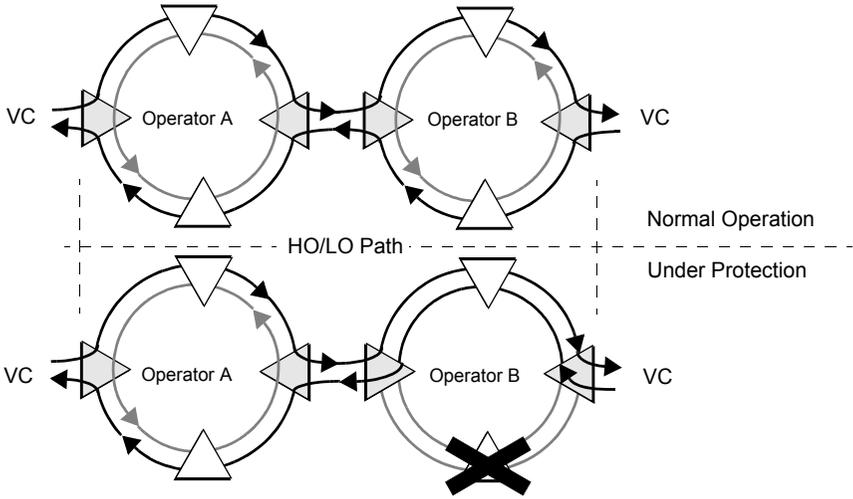


Figure 1.41 VC-P protection provides transport resilience across a tandem connection service.

AIS and LOP, non-intrusive information obtained from the POH, or client-layer information.

The SNC scheme can be used on any network topology. An example of a sub-network is a link between two DXCs with no path defined between them. The SNC can, in some cases, be the simplest method of protecting services across an interconnection (see Figure 1.42).

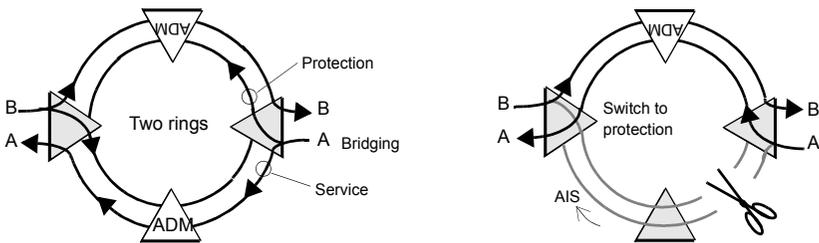


Figure 1.42 SNC-P is a dedicated protection mechanism. Traffic is sent simultaneously over both working and service lines. When a failure occurs, the far end switches to the alternative channel. Equivalent to SONET unidirectional path switched ring (UPSR).

SNC-P was the first ring protection scheme to be deployed and is still useful in access topologies, but it is probably not the best option for complex core networks.

1.14 OPERATION, ADMINISTRATION, AND MANAGEMENT

Operation, administration, and management (OAM) functions have been standardized by *telecommunications management networking* (TMN) in the ITU-T M.3000 recommendation series. TMN provides a framework for achieving a set of OAM services across heterogeneous networks.

The TMN defines a way of carrying out operation and maintenance tasks. It enables the center, often called *operation support system* (OSS), to communicate with the network elements of the installation.

There is a trend among operators to buy and install SDH from different vendors, because interoperation is guaranteed by transmission standards. This does not, however, mean that the management programs are compatible.

1.14.1 The TMN Standard

The TMN standard includes processes called *management entities* to manage the information. A management entity may take on one of two possible roles:

1. *Manager*: where it is the application that controls the network. It sends directives, and processes and stores the information received.
2. *Agent*: which is a process installed in the NE. Agents send responses that include information on performance, anomalies, and defects. They control both physical (switches, multiplexers, registers) and logical resources (multiplex section, paths, etc.) (see Figure 1.43).

1.14.1.1 Central management

The TMN describes the information exchange between management entities using the *open systems interconnection* (OSI) seven-layer model. The standard management includes:

- *Common management information protocol* (CMIP), which defines how the manager and the agent send and receive requests and responses. It is more robust, scalable, and secure than the protocol used in data communications the *simple network management protocol* (SNMP). However, its implementation is more complex.

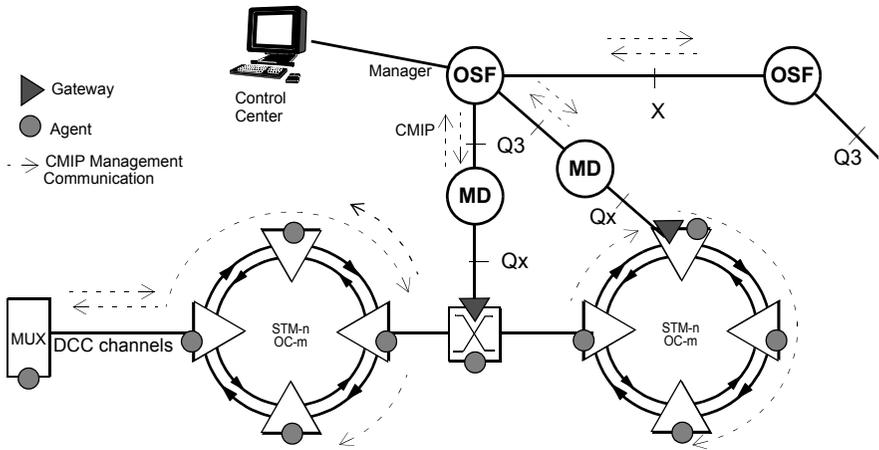


Figure 1.43 The transmission network is managed and monitored in a centralized way. The embedded DCC channels of section overheads (D1-D3 and D4-D12) allow the interchange of management information through the NE until the gateway which delivers it to the OSF. Agents, installed in the NE, provide information to the management system.

- *The Q interface*, which is the point of reference of CMIP where data is exchanged between the TMN operating system and the network elements. Q3 is defined for the *operation system functions* (OSF) and Qx for NE. A *mediation device* (MD) is usually in the middle. The data communication protocol at this point can be any of the following: Ethernet, X.25, ISDN, or TCP/IP.
- *The X interface*, which is used to communicate between two separate TMN systems.
- *Embedded channels*, which are used by the TMN to exchange information between entities. These channels are formed by STM/STS-frame Di-bytes (see Section 1.8.2). The TMN sends and receives management information across the network using the section overhead D-channels (see Figure 1.43).

NEs are manufactured with Qx interfaces to facilitate their integration into TMN architectures. The managed information itself, together with the rules by which it is presented and managed, is called the *management information base* (MIB).

1.14.2 TMN Benefits

The TMN has various benefits, including scalability, object-oriented management, and the fact that it does not require proprietary solutions. Operators can manage complex and dynamic SDH networks easily, while maintaining quality and protecting legacy investments. NEs have information exchange capabilities, using embed-

ded D_i channels that enable the OSF to reach to all the points of the network just by using a gateway. This means that the TMN does not need to link all the nodes, just one or a couple of gateways is enough to reach any agent installed in any NE.

The information gathered is the base on which to elaborate performance analysis that determines the *service level agreement* (SLA) control. The TMN provides comprehensive event information, making it easier to diagnose, troubleshoot, and repair the service. All of these are essential tasks for maintenance and operation.

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Chapter 5

Network Synchronization

Synchronization is the set of techniques that enable the frequency and phase of the equipment clocks in a network to remain constrained within the specified limits (see Figure 5.1). The first digital networks were asynchronous, and therefore did not call for properly working external synchronization. It was the arrival of SDH and SONET networks that started to make synchronization essential to maintain transmission quality and efficiency of supported teleservices.

Bad synchronization causes regeneration errors and *slips*. The effects of these impairments vary in different systems and services. Some isochronous¹ services, like telephony, tolerate a deficient synchronization rather well, and small or no effects can be observed by the end-user. Others, like digital TV transmission, fax, or compressed voice and video services, are more sensitive to synchronization problems. In HDLC, FRL, or TCP/IP types of data services, slips that occur force us to retransmit packets, and this makes transmission less efficient.

5.1 ARCHITECTURE OF SYNCHRONIZATION NETWORKS

Synchronization networks can have hierarchical or non-hierarchical architectures. Networks that use *hierarchical synchronization* have a tree architecture. In such networks a master clock is distributed, making the rest of the clocks slaves of its signal. A network with all the equipment clocks locked to a single master timing reference is called *synchronous*. The following elements can be found in the hierarchical synchronization network:

1. A *master clock*, which is usually an atomic cesium oscillator with global positioning system (GPS) and/or Loran-C² reference. It occupies the top of the pyramid, from which many synchronization levels spread out (see Table 5.1).

1. Isochronous (from the Greek "equal" and "time") pertains to processes that require timing coordination to be successful, such as voice and digital video transmission.
2. Loran-C is an electronic position fixing system using pulsed signals at 100 kHz.

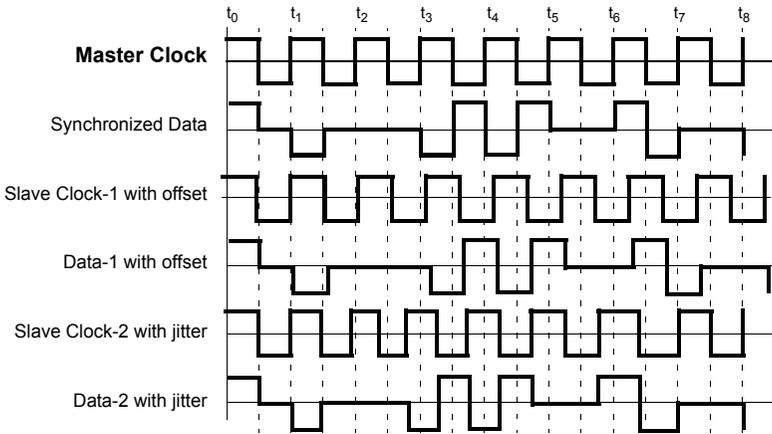


Figure 5.1 A master clock that marks the significant instances for data transmission. Clocks 1 and 2 are badly synchronized, and the data transmitted with these references is also affected by the same phase error.

2. High-quality *slave clocks*, to receive the master clock signal and, once it is filtered and regenerated, distribute it to all the NEs of their node.
3. *NE clocks*, which finish the branches of the tree by taking up the lowest levels of the synchronization chain. Basically, they are the ones using the clock, although they may also send it to other NEs.
4. *Links*, responsible for transporting the clock signal. They may belong to the synchronization network only, or, alternatively, form a part of a transport network, in which case the clock signal is extracted from data flow (see Figure 5.3).

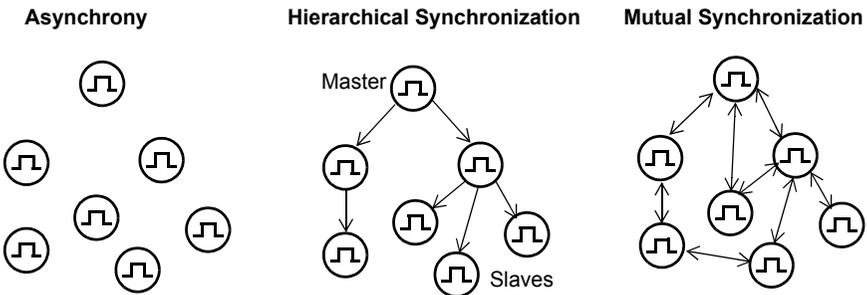


Figure 5.2 Classes of synchronization architectures.

The pure hierarchical synchronization architecture can be modified in several ways to improve network operation. *Mutual synchronization* is based on cooperation between nodes to choose the best possible clock. There can be several master clocks, or even a cooperative synchronization network, besides a synchronization protocol between nodes (see Figure 5.2). Bringing these networks into services is more complex, although the final outcome is very solid.

Those networks where different nodes can use a clock of their own, and correct operation of the whole depends on the quality of each individual clock, are called *asynchronous* (see Figure 5.2). Asynchronous operation can only be used if the quality of the node clocks is good enough, or if the transmission rate is reduced. The operation of a network (that may be asynchronous in the sense described above or not) is classified as *plesiochronous* if the equipment clocks are constrained within margins narrow enough to allow simple bit stuffing (see Figure 5.2).

General requirements for today's SONET and SDH networks are that any NE must have at least two reference clocks, of higher or similar quality than the clock itself. All the NEs must be able to generate their own synchronization signal in case they lose their external reference. If such is the case, it is said that the NE is in *hold-over*.

A synchronization signal must be filtered and regenerated by all the nodes that receive it, since it degrades when it passes through the transmission path, as we will see later.

Table 5.1
Clock performance.

<i>Type</i>	<i>Performance</i>
Cesium	From 10^{-11} up to 10^{-13}
Hydrogen	From 10^{-11} up to 10^{-13}
GPS	Usually 10^{-12}
Rubidium	From 10^{-9} up to 10^{-10}
Crystal	From 10^{-5} up to 10^{-9}

5.1.1 Synchronization Network Topologies

The synchronization and transport networks are partially mixed, since some NEs both transmit data and distribute clock signals to other NEs.

The most common topologies are:

1. *Tree*: This is a basic topology that relies on a master clock whose reference is

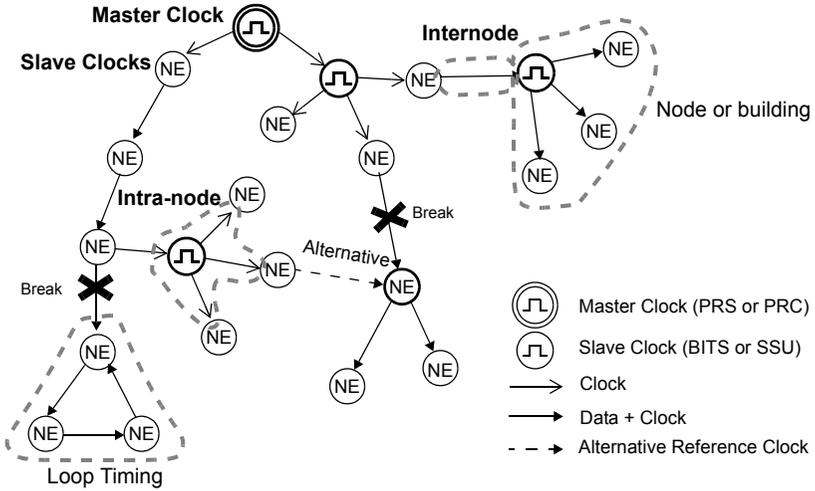


Figure 5.3 Synchronization network topology for SONET and SDH. This figure does not show links that are for transport only.

distributed to the rest of the slave clocks. It has two weak points: it depends on only one clock, and the signals gradually degrade (see Figure 5.5).

2. *Ring*: Basically, this is a tree topology that uses SDH/SONET ring configurations to propagate the synchronization signal. The ring topology offers a way to make a tree secure, but care must be taken to avoid the formation of synchronizing loops.
3. *Distributed*: Nodes make widespread use of many primary clocks. The complete synchronization network is formed by two or more islands; each of them depending on a different primary clock. To be rigorous, such a network is asynchronous, but thanks to the high accuracy of the clocks commonly used as a primary clock, the network operates in a very similar way to a completely synchronous network.
4. *Meshed*: In this topology, nodes form interconnections between each other, in order to have redundancy in case of failure. However, synchronization loops occur easily and should be avoided.

Synchronization networks do not usually have only one topology, but rather a combination of all of them. Duplication and security involving more than one master clock, and the existence of some kind of synchronization management protocol, are important features of modern networks. The aim is to minimize the problems associated with signal transport, and to avoid depending on only one clock in case of failure. As a result, we get an extremely precise, redundant, and solid synchronization network.

5.2 INTERCONNECTION OF NODES

There are two basic ways to distribute synchronization across the whole network:

- *Intranode*, which is a high-quality slave clock known as either *synchronization supply unit* (SSU) or *building integrated timing supply* (BITS). These are responsible for distributing synchronization to NEs situated inside the node (see Figure 5.3).
- *Internode*, where the synchronization signal is sent to another node by a link specifically dedicated to this purpose, or by an STM-*n*/OC-*m* signal (see Figure 5.3).

5.2.1 Synchronization Signals

There are several signals suitable for transporting synchronization:

- Analog, of 1,544 and 2,048 kHz;
- Digital, of 1,544 and 2,048 kbit/s;
- STM-*n*/OC-*m* line codes, from which one of the above-mentioned signals is derived, by means of a specialized circuit.

In any case, it is extremely important for the clock signal to be continuous. In other words, its mean frequency should never be less than its fundamental frequency (see Figure 5.4).

5.2.1.1 Clock transfer across T-carrier/PDH networks

These types of networks are very suitable for transmitting synchronization signals, as the multiplexing and demultiplexing processes are bit oriented (not byte oriented like SONET and SDH), and justification is performed by removing or adding single bits. As a result, T1 and E1 signals are transmitted almost without being affected by

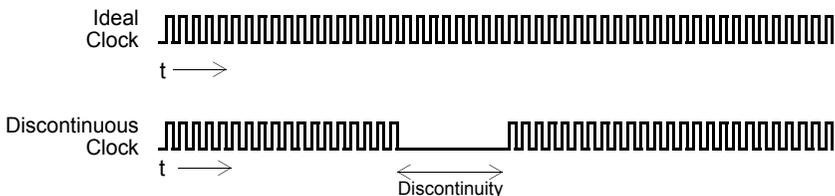


Figure 5.4 A pure clock signal is continuous, as, for example, the one provided by an atomic clock. A discontinuous signal in its turn could be a signal delivered by a T1 circuit transported in SONET.

justification jitter, mapping or overhead-originated discontinuities. This characteristic is known as *timing transparency*.

There is only one thing to be careful with, and that is to not let T1 and E1 signals cross any part of SONET or SDH, as they would be affected by phase fluctuation due to mapping processes, excessive overhead, and pointer movements. In short, T1 or E1 would no longer be suitable for synchronization.

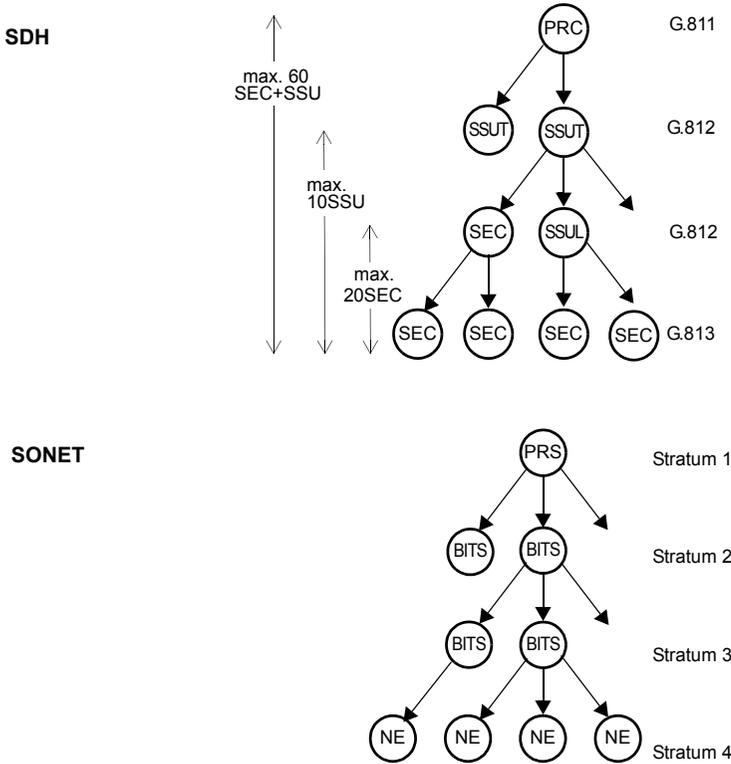


Figure 5.5 Synchronization network model for SONET and SDH. Stratum 3 has the minimum quality required for synchronizing an NE. In SDH the figures indicate the maximum number of clocks that can be chained together by one signal.

5.2.1.2 Clock transfer across SDH/SONET links

To transport a clock reference across SDH/SONET, a line signal is to be used instead of the tributaries transported, as explained before. The clock derived from an STM-*n*/OC-*m* interface is only affected by wander due to temperature and environ-

mental reasons. However, care must be taken with the number of NEs to be chained together, as all the NEs regenerate the STM-*n*/OC-*m* signal with their own clock and, even if they were well synchronized, they would still cause small, accumulative phase errors.

The employment of STM-*n*/OC-*m* signals has the advantage of using the S1 byte to enable *synchronization status messages* (SSMs) to indicate the performance of the clock with which the signal was generated (see Figure 5.6). These messages are essential in reconstructing the synchronization network automatically in case of failure. They enable the clocks to choose the best possible reference, and, if none is available that offers the performance required, they enter the holdover state.

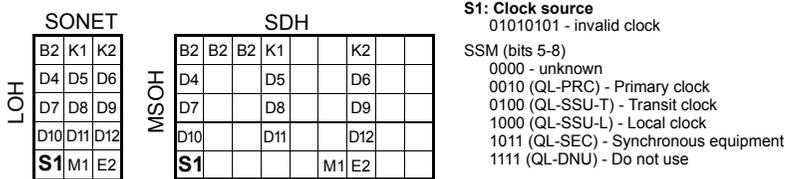


Figure 5.6 The S1 byte is used to send SSMs in SDH and SONET.

5.2.2 Holdover Mode

It is said that a slave clock enters holdover mode when it decides to use its own generator, because it does not have any reference available, or the ones available do not offer the performance required. In this case, the equipment remembers the phase and the frequency of the previous valid reference, and reproduces it as well as possible. Under these circumstances, it puts an SSM=QL-SEC message into the S1 byte of STM-*n*/OC-*m* frames, and, if it was generating synchronization signals at 1.5 or 2 MHz, it stops doing so.

5.2.3 Global Positioning System

The *global positioning system* (GPS) is a constellation of 24 satellites that belongs to the U.S. Department of Defense. The GPS receivers can calculate, with extreme precision, their terrestrial position and the universal time from where they extract the synchronization signal. The GPS meets the performance required from a primary clock (see Table 5.1). However, the GPS system might get interfered with intentionally, and the U.S. Department of Defense reserves the right to deliberately degrade its performance for tactical reasons.

5.3 DISTURBANCES IN SYNCHRONIZATION SIGNALS

Since synchronization signals are distributed, degradation in the form of jitter and wander accumulate. At the same time they are affected by different phenomena that cause phase errors, frequency offset, or even the complete loss of the reference clock. Care must be taken to avoid degradation in the form of slips and bit errors by filtering and an adequate synchronization distribution architecture (see Figure 5.7).

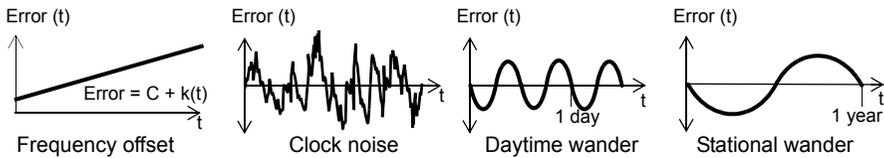


Figure 5.7 Sources of phase variation.

5.3.1 Frequency Offset

Frequency offset is an undesired effect that occurs during the interconnection of networks or services whose clocks are not synchronized. There are several situations where frequency deviations occur (see Figure 5.8):

- On the boundary between two synchronized networks with different primary reference clocks;
- When tributaries are inserted into a network by non-synchronized ADMs;
- When, in a synchronization network, a slave clock becomes disconnected from its master clock and enters holdover mode.

5.3.1.1 Consequences of frequency offset in SDH/SONET

To compensate for their clock differences, SDH/SONET networks use pointer adjustments. Let us think of two multiplexers connected by STM-1 (see Figure 5.8), where ADM2 is perfectly synchronized, but ADM1 has an offset of 4.6 parts per million (ppm).

$$f_1 = 155,52Mbps$$

$$f_2 = 155,52Mbps + 4,6ppm = 155,52\left(1 + \frac{4,6}{10^6}\right)Mbps$$

ADM1 inserts a VC-4, but as ADM2 uses another clock, it should carry out pointer adjustments periodically, to compensate for the difference between the two clocks.

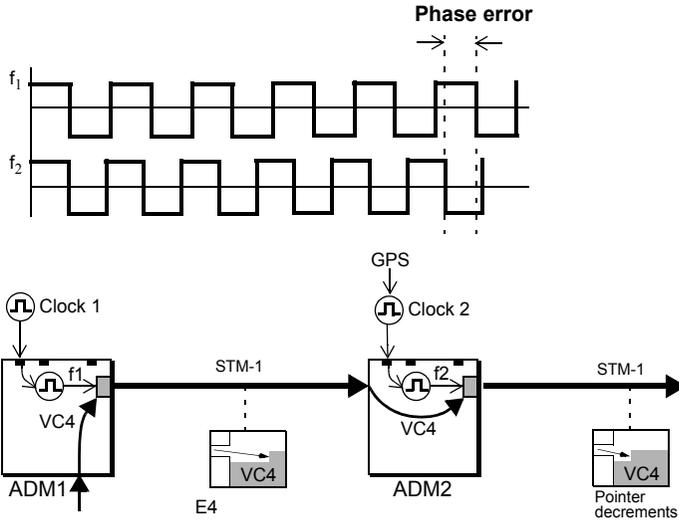


Figure 5.8 Comparison of two reference signals that synchronize two SDH multiplexers. Periodical pointer adjustment occurs due to the frequency offset there is between the two signals.

That is to say, a 4.6 ppm frequency in STM-1 equals to:

$$f_3 = f_2 - f_1 = 155,52 \left(1 + \frac{4,6}{10^6} \right) - 155,52 \quad \text{Mbps}$$

$$f_3 = (155,52 \cdot 10^6) \left(1 + \frac{4,6}{10^6} - 1 \right) = 155,52 \times 4,6 = 715,4 \quad \text{bps}$$

However, this difference does not affect the whole STM-1 frame, but only the VC-4, and therefore we will only consider the difference of size between the two:

$$R = (VC4)_{bytes} / (STM1)_{bytes} = 261 / 270 = 0,96$$

$$f_d = f_3 \times R = 691,5 \text{ bps}$$

A pointer movement, here, is a decrement of 3 bytes that makes it possible to fit 24 more bits from VC-4 in the STM-1 frame. The adjustment period is:

$$T_{ptr} = \text{Decrement}_{bits} / f_d = 24_{bits} / 691,5_{bps}$$

$$T_{ptr} = 34,7 \times 10^{-3} \text{ s}$$

That is, ADM2 decrements the AU-4 pointer every 34.7 ms to compensate for the ADM1 drift (see Figure 5.9).

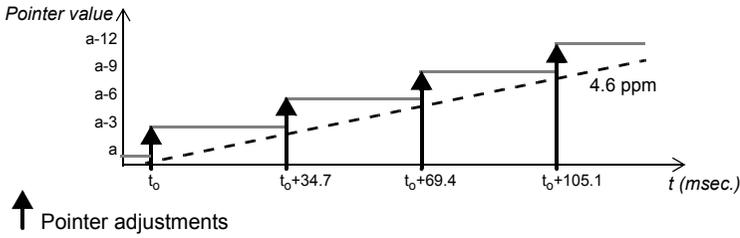


Figure 5.9 The position of the VC-4 container drifts, due to AU pointer adjustments to compensate for the differences between the two clocks.

5.3.2 Phase Fluctuation

In terms of time, the phase of a signal can be defined as the function that provides the position of any significant instant of this signal. It must be noticed that a time reference is necessary for any phase measurement, because only a phase relative to a reference clock can be defined. A significant instant is defined arbitrarily; it may for instance be a trailing edge or a leading edge, if the clock signal is a square wave (see Figure 5.10).

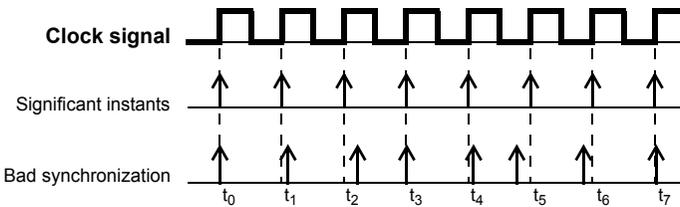


Figure 5.10 Phase error of a signal in relation to its ideal frequency.

Here, when we talk about a phase, we think of it as being related to clock signals. Every digital signal has an associated clock signal to determine, on reception, the instants when to read the value of the bits that this signal is made up of. The clock recovery on reception circuits reads the bit values of a signal correctly when there is no phase fluctuation, or when there is very little. Nevertheless, when the clock recovery circuitry cannot track these fluctuations (absorb them), the sampling instants of the clock obtained from the signal may not coincide with the correct instants, producing bit errors.

When phase fluctuation is fast, this is called jitter. In the case of slow phase fluctuations, known as wander, the previously described effect does not occur.

Phase fluctuation has a number of causes. Some of these are due to imperfections in the physical elements that make up transmission networks, whereas others result from the design of the digital systems in these networks.

5.3.2.1 Jitter

Jitter is defined as short-term variations of the significant instants of a digital signal from their reference positions in time, ITU-T Rec. G.810 (see Figure 5.11). In other words, it is a phase oscillation with a frequency higher than 10 Hz. Jitter causes sampling errors and provokes slips in the *phase-locked loops* (PLL) buffers (see Figure 5.12). There are a great many causes, including the following:

Jitter in regenerators

As they travel along line systems, SONET and SDH signals go through a radio-electrical, electrical, or optical process to regenerate the signals. But clock recovery in regenerators depends on the bit pattern transported by the signal, and the quality of the recovered clock becomes degraded if transitions in the pattern are distributed heterogeneously, or if the transition rate is too low. This effect can be countered by means of scrambling, which is used to destroy correlation of the user-generated bit sequence. The most commonly used line codes add extra transitions in the pattern, to allow proper clock recovery at the receiving end.

Moreover, this type of jitter is accumulative, which means that it increases together with the increase in the number of repeaters looked at.

Jitter due to mapping/demapping

Analog phase variation in tributary signals is sampled and quantized when these are multiplexed in a higher-order signal. This is an inherent mechanism in any TDM system. In SDH, for instance, every 125 μs , certain bytes of the phase are available for adjusting the phase. In short, the phase of tributary signals is quantized.

Also, a tributary signal may be synchronized with a different clock than the clock used to synchronize the aggregate signal that will carry it. The above situations give rise to *phase justification*: Bits of the tributary signal are justified, to align them with the phase of the aggregate signal frame; that is, creating jitter.

Pointer jitter

The use of pointers in SDH/SONET makes it possible to discard the effects of bad synchronization, but these pointer movements provoke an extensive phase fluctuation. Pointer movements are equal to discontinuities in the transported tributaries.

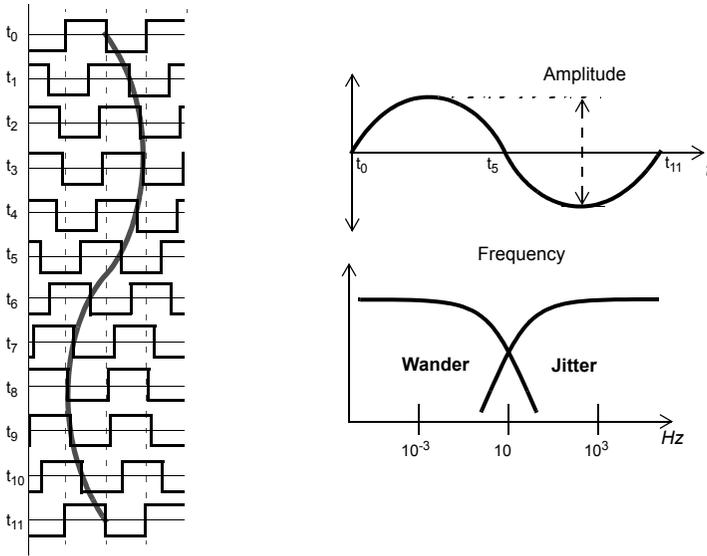


Figure 5.11 A phase fluctuation of a signal is an oscillating movement with an amplitude and a frequency. If this frequency is more than 10 Hz, it is known as jitter, and when it is less than that, it is called wander.

Once the tributary has been extracted, the PLL circuit must continuously adapt itself to bit flows. If the VC-4 pointer has incremented in an STM-1, it will receive 24 bits less, and it must slow down to maintain a constant level for its buffer. If by contrast it has decremented, it will receive 24 bits more and should accelerate. As a result, the extracted tributary will contain jitter.

5.3.2.2 Wander

Wander is defined as long-term variations of the significant instants of a digital signal from their reference positions in time (ITU-T Rec. G.810). Strictly speaking, wander is defined as the phase error comprised in the frequency band between 0 and 10 Hz of the spectrum of the phase variation. Wander is difficult to filter when crossing the *phase-locked loops* (PLLs) of the SSUs, since they hardly attenuate phase variations below 0.1 Hz. This is because slow phase variations get compensated with pointer adjustments in SDH/SONET networks, which is one of the main causes of jitter (see Figure 5.11).

Wander brings about problems in a very subtle way in a chained sequence of events. First, it causes pointer adjustments, which are then reflected in other parts of the network in the form of jitter. This in its turn ends up provoking slips in the output buffers of the transported tributary.

The following are the most typical causes of wander:

Changes in temperature

Variations between daytime and nighttime temperature, and seasonal temperature changes have three physical effects on transmission media:

- There are variations in the propagation rate of electrical, electromagnetic or optical signals.
- There is variation of length, when the medium used is a cable (electrical or optical), due to changes between daytime and nighttime or winter and summer.
- There is different clock behavior when temperature changes occur.

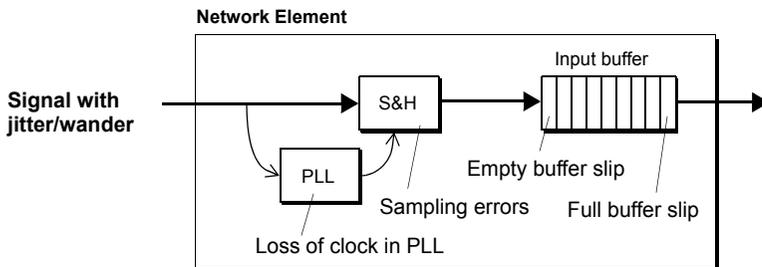


Figure 5.12 Jitter and wander affect every stage of data recovery, producing a number of sampling errors, clock, losses, and overflow.

Clock performance

Clocks are classified according to their average performance in accuracy and offset. The type of resonant oscillator circuit used in the clock source and the design of its general circuitry both add noise, and this results in wander.

5.4 SYNCHRONIZATION OF TRANSMISSION NETWORKS

T-carrier and PDH networks have their first hierarchy perfectly synchronous. In E1 and DS1 frames, all the channels are always situated in their own time slots. The rest of the hierarchical multiplexing levels are not completely synchronous, but frequency differences can be accommodated by the bit stuffing mechanism.

T-carrier and PDH nodes do not need to be synchronized, since each of them can maintain their own clock. The only requirement is that any clock variations must

be kept within the specified limits, so that the available justification bits can be fitted in without problems caused by clock differences.

Table 5.2
Stratum timing accuracy.

<i>Stratum</i>	<i>Identifier</i>	<i>Accuracy</i>	<i>Drift</i>
1	ST1	1×10^{-10}	2.523/year
2	ST2	1.6×10^{-8}	11.06/day
3	ST3	4.6×10^{-6}	132.48/hour
4	ST4	3.2×10^{-5}	15.36/minute

5.4.1 Synchronization in SONET and SDH

In SONET and SDH, the NEs must be synchronized to reduce pointer movements to a minimum. Pointer movements, as we have seen, are a major cause of jitter. The synchronization network follows a master-slave hierarchical structure:

- *Primary reference clock*, in SDH, or *primary reference source*, in SONET: This is the one that provides the highest quality clock signal. It may be a cesium atomic clock, or a *coordinated universal time* (UTC) signal transmitted via the GPS system.
- *Synchronization supply unit*, in SDH, or *building integrated timing supplies*, in SONET: This clock takes its reference from the PRC and provides timing to the switching exchanges and NEs installed in the same building (it is also known as *building synchronization unit*) or on the same premises. It is usually an atomic clock, although not of such a high quality as the PRC.
- *Synchronous equipment clock* (SEC): This clock takes its reference from an SSU, although it is of lower quality (for example, quartz). It is the internal clock of all the NEs (multiplexer, ADM, etc.).

Whereas a PRC/PRS clock is physically separate from the SDH/SONET network, an SSU/BITS clock may be a separate piece of equipment, in which case it is called a *stand-alone synchronization equipment*, or it may be integrated into an NE (DXC or multiplexer). By definition, an SEC is integrated into an NE. The timing between clocks is transmitted by SDH/SONET sections (STM-*n*/OC-*m*) or PDH/T-carrier paths (2 or 1.5 Mbit/s) that can cross various intermediary PDH/T-carrier multiplexing stages, and various PDH/T-carrier line systems. The interfaces for these clocks are 2 or 1.5 Mbit/s, 2 or 1.5 MHz and STM-*n*/OC-*m*, and their presence or absence depends on the specific implementation of the device.

5.4.1.1 SONET synchronization network

In a SONET synchronization network, the master clock is called *primary reference source* (PRS), whereas slave clocks are building integrated timing supply (BITS) that end up synchronizing the NEs. The GR-1244-CORE specifies the rules and performance margins for both PRS and BITS.

BITS synchronizes the network equipment, and it is also used by switches. The performance required to synchronize a node is Stratum 3 (see Table 5.2).

5.4.1.2 SDH synchronization network

In an SDH synchronization network, the master clock is called *primary reference clock* (PRC), whereas *synchronization supply units* (SSUs) are slave clocks and the NE is a *synchronous equipment clock* (SEC). All of them must be kept inside the performance margins defined by the corresponding recommendations (see Table 5.3).

Table 5.3
SDH timing accuracy.

<i>Use</i>	<i>Accuracy</i>	<i>Drift</i>	<i>ITU-T</i>
PRC	1×10^{-11}	—	G.811
SSU-T	5×10^{-10}	$10 \times 10^{-10}/\text{day}$	G.812
SSU-L	5×10^{-8}	$3 \times 10^{-7}/\text{day}$	G.812
SEC	4.6×10^{-6}	$5 \times 10^{-7}/\text{day}$	G.813

5.4.2 Synchronization Models

In SDH/SONET networks, there are at least four ways to synchronize the add and drop multiplexers (ADM) and *digital cross connects* (DXC) (see Figure 5.13):

1. *External timing*: The NE obtains its signal from a BITS or *stand-alone synchronization equipment* (SASE). This is a typical way to synchronize, and the NE usually also has an extra reference signal for emergency situations.
2. *Line timing*: The NE obtains its clock by deriving it from one of the STM-*n*/OC-*m* input signals. This is used very much in ADM, when no BITS or SASE clock is available. There is also a special case, known as *loop timing*, where only one STM-*n*/OC-*m* interface is available.
3. *Through timing*: This mode is typical for those ADMs that have two bidirectional STM-*n*/OC-*m* interfaces, where the Tx outputs of one interface are syn-

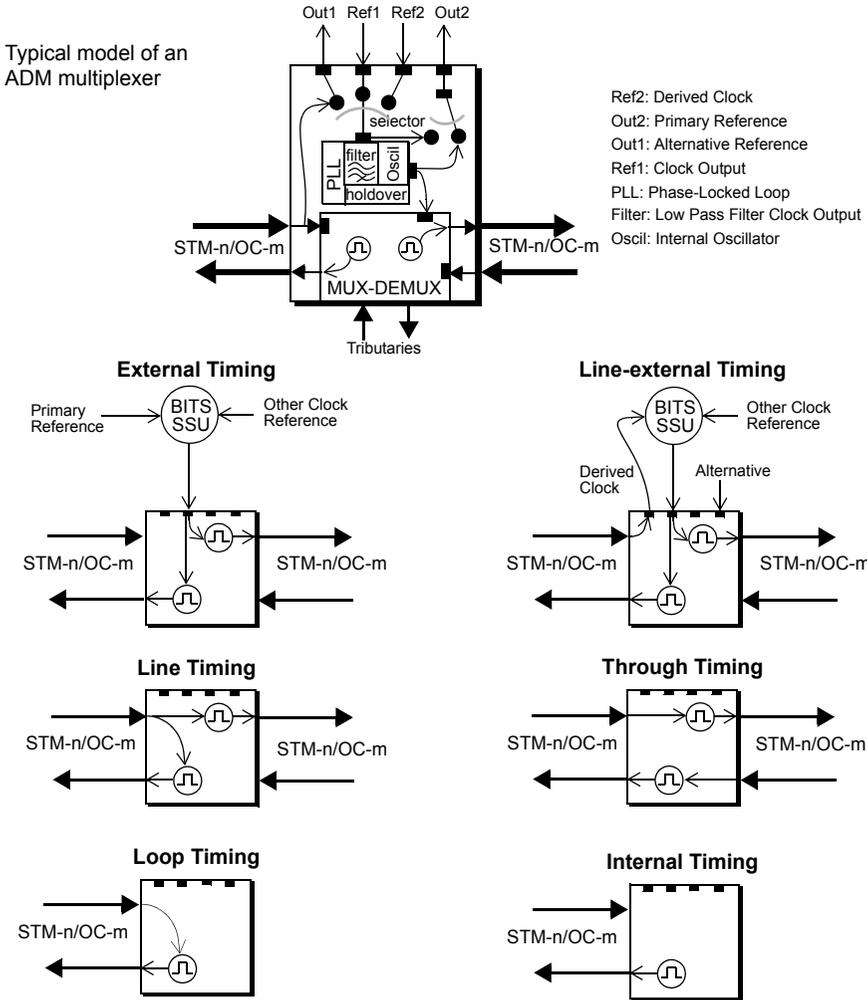


Figure 5.13 Synchronization models of SDH/SONET network elements.

chronized with the Rx inputs of the opposite interface.

4. *Internal timing*: In this mode, the internal clock of the NE is used to synchronize the STM-n/OC-m outputs. It may be a temporary holdover stage after losing the synchronization signal, or it may be a simple line configuration where no other clock is available.

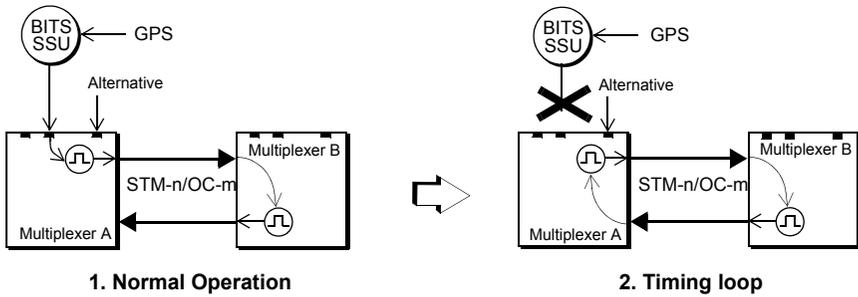


Figure 5.14 A synchronization pitfall. The multiplexer A, when left without a reference, should have remained in holdover state, if it did not have another clock signal. Generally, secondary clock references should not be taken in line timing synchronization.

5.4.3 Timing Loops

A timing loop is in bad synchronization when the clock signal has closed itself, but there is no clock, either master or slave, that would autonomously generate a non-deficient clock signal. This situation can be caused by a fault affecting an NE in such a way that it has been left without a reference clock, and therefore it has chosen an alternative synchronization: a signal that has turned out to be the same signal, returning by another route (see Figure 5.14). A synchronization loop is a completely unstable situation that may provoke an immediate collapse of part of the network within the loop.

The ring network synchronization chain should avoid a synchronization loop (see Figure 5.15).

5.5 DIGITAL SYNCHRONIZATION AND SWITCHING

Digital switching of $n \times 64$ -kbit/s channels implies that the E1 and T1 frames must be perfectly aligned to make it possible to carry out channel exchange (see Figure 5.16).

The frames are lined by means of a buffer in every input interface of a switch. The bits that arrive at f_i frequency get stored in them, to be read later at the frequency used by the switch, f_o .

But if the clocks are different, $|f_i - f_o| > 0$, the input buffer sooner or later ends up either empty or overloaded. This situation is known as a *slip*: If the buffer becomes empty, some bytes are repeated, whereas if the buffer is overloaded, some valid bits must be discarded in order to continue working. That is to say, slips are

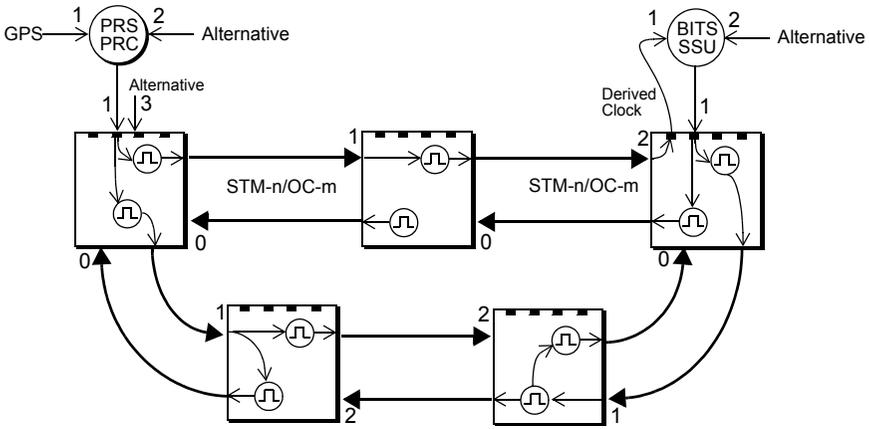


Figure 5.15 The ring network synchronization chain. “1” is the primary reference, “2” and “3” are alternative clocks, and “0” is to avoid a synchronization loop.

errors that occur when PLLs cannot adapt themselves to clock differences or phase variations in frames.

$$f_d = 86,000 \times |f_i - f_o| / n \quad (\text{slips/day})$$

where
 86,400 is number of seconds per day
 n: bits repeated or discarded per slip
 f_i = input bit rate
 f_o = output bit rate

When effects are caused by slips:

- In the *voice* they are usually not noticed; a click may be noticed when voice is sent compressed;
- In a *facsimile* they may damage many text lines;
- In *modems* they cause microbreaks and may sometimes break the whole connection;
- In *digital TV*, there is loss of color or frame synchronization;
- In *data networks* like SNA, HDLC, frame relay, TCP/IP, there is loss of performance.

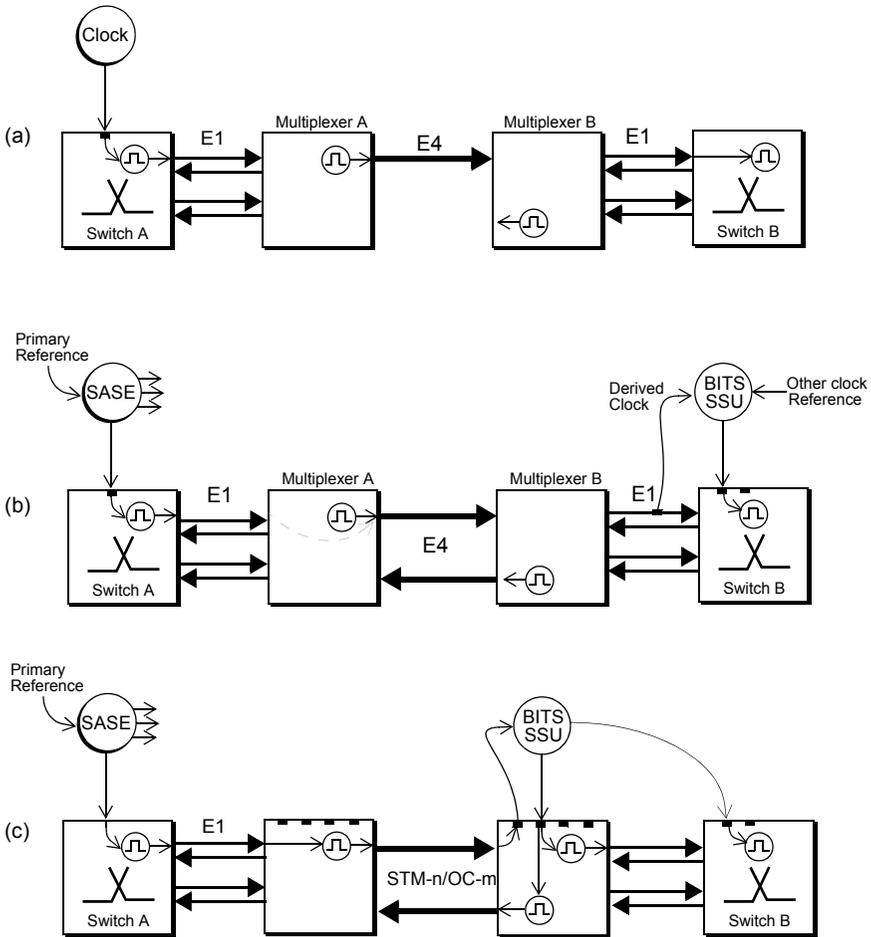


Figure 5.16 Synchronization of two digital centrals: (a) by signal derived from the PDH chain; (b) by PDH and SASE chain; and (c) across SDH network.

5.6 SSU IN A SYNCHRONIZATION NETWORK

The SSU is in charge of synchronizing all the NEs of its node. It has many alternative clock inputs or references, to confront possible clock signal losses. It may be integrated in an ADM or CXC multiplexer, or it can be a stand-alone equipment, in which case it is known as SASE (see Figure 5.17).

Depending on their performance, there are two types of SSUs:

- *Synchronization supply unit transit* (SSU-T): These are of higher quality and they are used to synchronize NEs, or as references for other SSUs.
- *Synchronization supply unit local* (SSU-L): These are of lower quality, and they only synchronize the NEs of their own node.

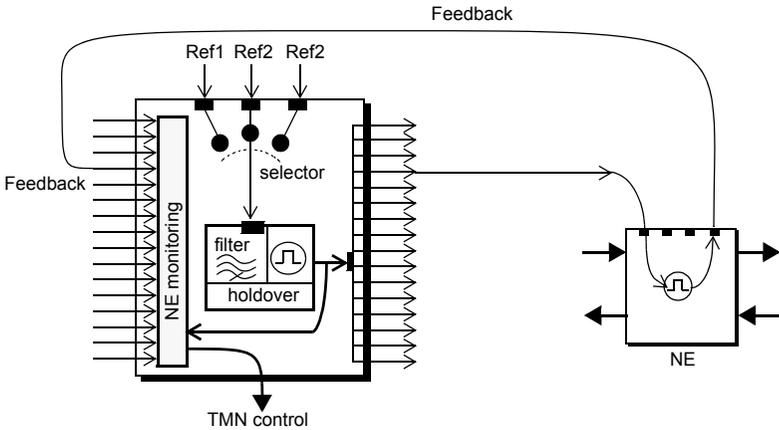


Figure 5.17 Diagram of an SSU function model.

5.6.1 Functions of SSU

An SSU has many functions, and they can be described as follows:

1. The SSU accepts many clock references, tests their performance and selects one of them, filtering it from noise and other interference.
2. It sends the signal chosen to an internal oscillator that acts as a reference to generate a new synchronization signal.
3. The new signal is distributed between all the NEs of its node, and it may also be sent to another SSU in another node.
4. If the reference chosen starts to degrade or is lost, the SSU should switch to one of its alternative references.
5. If no valid reference is found, the SSU enters holdover mode, generating a clock of its own that emulates the characteristics of the previous valid reference.

In the case of an SASE, there are other functions as well:

1. It monitors the synchronization status of the NEs of its node by means of return links.
2. It continuously informs the TMN control level of both its own synchronization status and that of the NEs of its node.

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Chapter 3

Jitter and Wander Control

3.1 DEALING WITH JITTER

Jitter is one of the three traditionally considered effects that disturb the timing of networks: *jitter*, *wander*, and *slips*. The first two are variations of the same physical effect: phase fluctuation. Slips are a different phenomenon, although related to the above.

3.1.1 Phase Fluctuation

In terms of time, the phase of a signal can be defined as the function that provides the position of any significant instant of this signal relative to its origin in time. A significant instant is defined arbitrarily; for instance, it may be a trailing edge or leading edge, if the signal is a square wave (clock signal).

Here, when we talk about a phase, we think of it as being related to clock signals. Every digital signal has an associated clock signal in order to determine, on reception, the instants at which to read the value of the bits this signal is made up of. The clock recovery on reception circuits reads the bit values of a signal correctly when there is no phase fluctuation or when there is very little. Nevertheless, when the phase fluctuation, presented by the signal received is fast enough, due to technological limitations, the circuits may not be able to trace these fluctuations (absorb them). It is in such cases that the sampling instants of the clock obtained from the signal may not coincide with the correct instants, producing bit anomalies.

When phase fluctuation is fast, this is called jitter. In the case of slow phase fluctuations, known as wander, the previously described effect does not occur. Random pointer adjustments do occur, however, and may be the cause of jitter in the tributary signals carried by the synchronous signals.

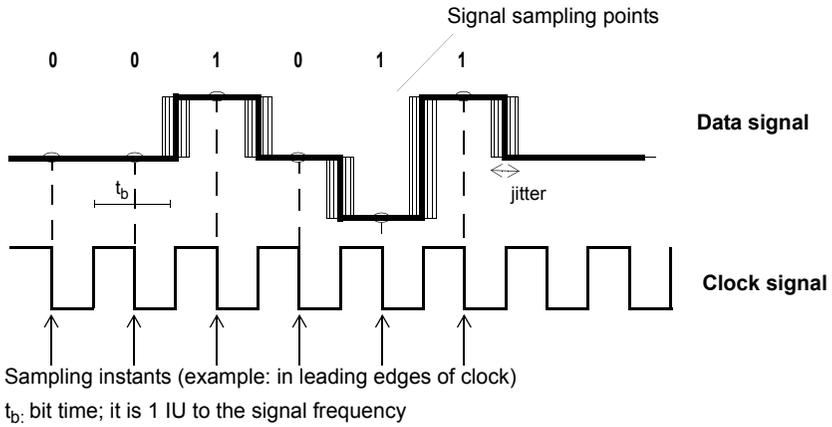


Figure 3.1 Definition of unitary interval.

3.1.2 Jitter Metrics and Measurement

The parameters that characterize the jitter of a digital signal are amplitude and frequency. The amplitude quantifies the extent to which a significant instant deviates from its ideal reference position. The frequency tells us how quickly this significant instant is moving relative to its ideal position in time.

If we look at the amplitude of phase fluctuation with time as a periodic signal, when its frequency is higher than 10 Hz, the fluctuation is said to be fast, and this is jitter. Phase fluctuation is not usually a periodic signal in real cases, and for this reason we analyze the presence of frequency components in its spectrum above or below 10 Hz, to determine if what we have is jitter or wander.

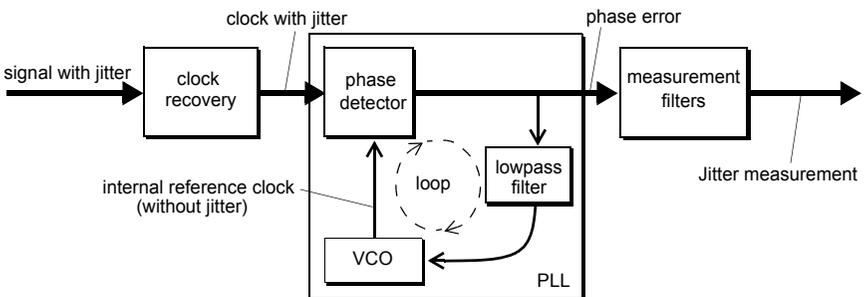


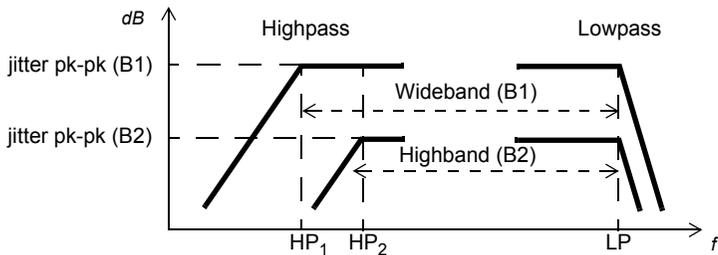
Figure 3.2 The jitter measurement does not need an external reference clock because it is recovered from the incoming signal to be tested.

3.1.2.1 Unitary interval

It is usual to measure jitter amplitude in terms of a relative unit. This unit is normalized in respect to the signal rate, and is called a unitary interval (UI). A unitary interval is defined as the time equivalent to the bit time for the work rate in question (see Figure 3.1). Thus, a unitary interval for a 2-Mbps signal corresponds to approximately 488×10^{-9} s, whereas a UI for an STM-1 signal corresponds to 6.4 ns.

3.1.2.2 Jitter measurement filters

The simplest jitter measurements have the goal of obtaining peak-to-peak amplitude values in UI within a specific frequency band over a specific measurement interval (see Figure 3.2). This means that any instrument capable of measuring these fluctuations must have a bank of weighting filters that limit the band of the signal measured. These filters (in terms of their frequency cut-offs and slopes) are defined by ITU-T recommendations.



Rate	B ₁	B ₂	Rate	HP ₁	HP ₂	LP
64 Kbps	0.25	0.05	64 Kbps	20 Hz	3 kHz	20 kHz
2 Mbps	1.5	0.2	2 Mbps	20 Hz	18 kHz	100 kHz
8 Mbps	1.5	0.2	8 Mbps	20 Hz	3 kHz	400 kHz
34 Mbps	1.5	0.15	34 Mbps	100 Hz	10 kHz	800 kHz
140 Mbps	1.5	0.075	140 Mbps	200 Hz	10 kHz	3,500 kHz

Figure 3.3 Jitter measurement filters for PDH and maximum jitter values in line with G.823.

ITU-T Rec. G.823 establishes the levels of jitter that can be found in PDH interfaces, from 64 Kbps to 140 Mbps (see Figure 3.3). In the same way, Telcordia GR-499 deals with the jitter related to T-carrier 1.5 and 45 Mbps interfaces. Two measurement filters are specified:

- *Wideband*: This filter measures jitter over the whole band of frequencies on which phase fluctuation is thought to exist, and the band depends on the specif-

ic hierarchical interface. This filter is specified between the frequencies HP1 and LP (highpass filter and lowpass filter, respectively).

- *Highband*: This filter allows us to characterize the spectral distribution of the high frequency jitter, which is the jitter most likely to cause problems in clock recovery circuits.

As with PDH or T-carrier, measurement filters are established for SDH and SONET; this time according to ITU-T Rec. G.825 (SDH) and ANSI T1.105.03, ANSI T1.102, and Telcordia GR-253 (SONET). In this case, a highband and a wideband filter are also defined. (see Figure 3.4).

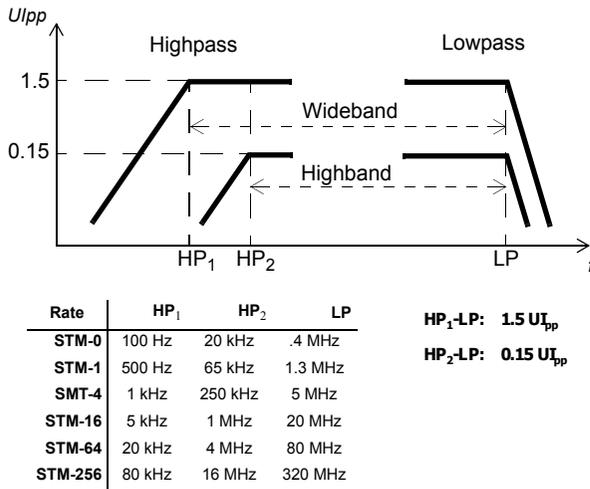


Figure 3.4 Jitter measurement filters and maximum jitter values for SDH, in line with G.825.

In short, weighting the measurement using filters serves to determine the spectral content of jitter in each frequency band (pass bands of the programmed filters). These weightings allow conclusions to be drawn when problems appear, or even enable us to predict them. For instance, a concentration of energy in a specific low frequency band may result in specific synchronization problems, or problems in operating the terminal equipment.

3.1.2.3 Measurement interval

As mentioned before, a jitter amplitude measurement must be carried out over a given measurement interval. The usual measurement period is 60 seconds, although when measuring jitter, longer periods are required due to pointer adjustments (phase quantization), as these occur sporadically (see Figure 3.5).

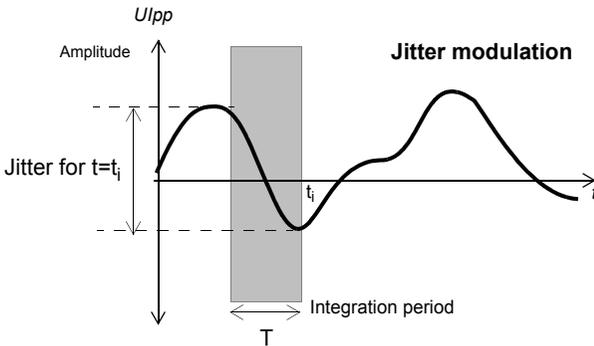


Figure 3.5 The integration period is the time interval measuring the jitter.

3.1.3 Measuring Jitter in Output Interfaces

This measurement attempts to obtain the jitter amplitude (expressed in UIs) present in the output port of a specific NE. The ITU-T specifies and limits the maximum amount of jitter allowed in a network. In particular, ITU-T Rec. G.825 (SDH) and G.823 (PDH), and Telcordia GR-253 (SONET) and GR-499 (T-carrier), limit the maximum amount of jitter in the NE output ports. This output jitter may be generated by the NE itself, or may result from the transfer of jitter from one of the inputs of the element, either the data input or the synchronization input. The result of the measurement is the jitter amplitude in a specific bandwidth, specified by the above-mentioned recommendations for each rate in the PDH and SDH hierarchies (see Figure 3.6). Should we wish to measure the jitter generated by the NE, we need to connect an input signal free of jitter.

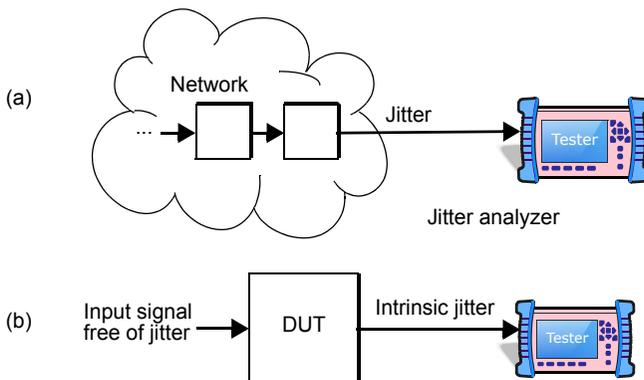


Figure 3.6 (a) Jitter in output port: General case.
 (b) Intrinsic jitter. DUT is the NE being examined.

3.1.4 Measuring Jitter Tolerance

Network elements are designed to tolerate a certain amount of jitter in their inputs without losing synchronization or introducing anomalies. This amount is specified in Recommendations ITU-T Rec. G.823 (PDH), and G.958 and G.825 for SDH, and Telcordia GR-499 (T-carrier), and GR-253 (SONET).

Jitter tolerance is therefore defined as the maximum jitter amplitude in the input of an NE that does not produce bit anomalies or synchronization anomalies. These amounts are specified by the recommendations in the form of masks. In these masks, jitter amplitude is specified in UI versus frequency. It is recommended that the measurement configuration be synchronized with a reference clock common to both the NE and the tester, to avoid occasional pointer adjustments. The input signal in which jitter is to be introduced must be a pattern that is suitable for the frame rate of the signal (see Figure 3.7). The pattern depends on its rate (for instance, those stipulated by ITU-T Rec. O.150 for PDH, or O.181 test structures for SDH).

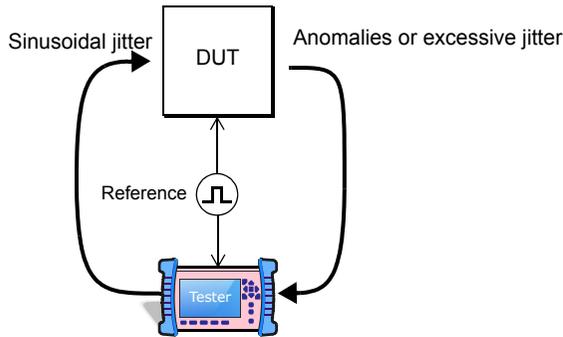


Figure 3.7 Jitter tolerance measurement configuration.

The type of NE examined determines which input and output interfaces come into play for the measurement being performed:

- *Regenerators*: Measurements are made in the output line interface corresponding to the input line interface where jitter is inserted.
- *Multiplexers*: Measurements are made on the channel, in the output aggregate signal corresponding to the input interface where jitter is inserted.
- *Demultiplexers*: Any tributary interface is representative of the aggregate input interface where jitter is inserted.

More precisely, the measurement is carried out by inserting sinusoidal jitter in an input port. The amplitude of the jitter tone introduced is increased until events are measured at the output port. This is repeated at set frequencies. There are two ways to carry out the tolerance measurement: onset of errors and BER penalty.

3.1.4.1 Onset of errors

This is the usual method for checking that the buffering and clock recovery functions are working properly in the NEs. It consists of increasing the jitter amplitude until we can observe the signal deteriorating to the point where it reaches a certain threshold (for instance, the threshold recommended by O.171 for PDH signals is two seconds with anomalies in a period of 30 seconds). At this point, the jitter amplitude is registered, and this gives us the tolerance to this frequency. The test is then repeated for a set range of frequencies.

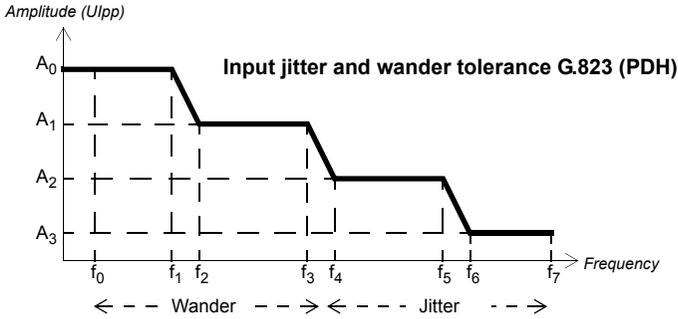
3.1.4.2 BER penalty

This method is more appropriate for line systems (regenerators), normally using optical interfaces. In this case, the tolerance level is established when the deterioration of the signal is the same as that produced by lowering the transmission power by 1 dB. In other words, if the anomaly rate produced for a set amplitude of sinusoidal jitter coincides with that measured when the power is lowered by 1 dB, this amplitude is the jitter tolerance for that frequency. The test is then repeated for a set range of frequencies.

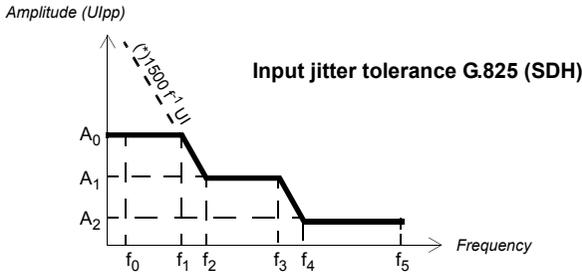
3.1.4.3 Tolerance masks

Jitter tolerance measurements are aimed at checking that certain limits of jitter amplitude, preestablished by ITU-T and Telcordia recommendations for a set range of frequencies, are not exceeded. These limits are shown in masks or amplitude-frequency graphs in Recommendations ITU-T Rec. G.823 (PDH) and G.825 (SDH), and Telcordia GR-499 (T-carrier), and GR-253 (SONET). The masks show the frequencies at which tolerance should be measured (see Figure 3.8).

For optical regenerators in SDH networks, ITU-T Rec. G.958 likewise defines tolerance values by means of two masks: one for A-type and another one for B-type devices. The mask for A-type devices complies with ITU-T Rec. G.825, while the mask for B-type devices is much more restrictive (see Figure 3.9).



Rate	A ₀ (μs)	A ₁ (μs)	A ₂ (UI)	A ₃ (UI)	f ₀ (μH)	f ₁ (mH)	f ₂ (mH)	f ₃ (Hz)	f ₄ (Hz)	f ₅ (Hz)	f ₆ (kHz)	f ₇ (kHz)
64 Kbps	18	-	0.5	0.05	12	-	-	4.33	20	600	3	20
2 Mbps	18	8.8	1.5	0.2	12	4.88	10	1.7	20	2400	18	100
8 Mbps	-	-	1.5	0.2	-	-	-	-	20	400	3	400
34 Mbps	4	1	1.5	0.15	10000	32	130	4.4	100	1000	10	800
140 Mbps	4	1	1.5	0.075	10000	32	130	2.2	200	500	10	3500



Rate	A ₀ (UI)	A ₁ (UI)	A ₃ (UI)	f ₀ (H)	f ₁ (H)	f ₂ (kHz)	f ₃ (kHz)	f ₄ (kHz)	f ₅ (MH)
STM-1e	38.9	1.5	0.075	10	19.3	0.5	3.3	65	1.3
STM-1o	38.9	1.5	0.15	10	19.3	0.5	6.5	65	1.3
STM-4	see *	1.5	0.15	9.65	1000	1	25	250	5
STM-16	622	1.5	0.15	10	12.1	5	100	1000	20
STM-64	2490	1.5	0.15	10	12.1	20	400	4000	80

Figure 3.8 Input jitter and wander tolerance, G.823 and G.825

3.1.5 Measuring Jitter Transfer

Network elements have a limited capacity to eliminate the jitter that may occur in their input ports. To evaluate this filtering capacity, the function of jitter transfer is to define the relation between the jitter amplitudes on input and output for a set range of frequencies. As usual in transfer functions, this relation of amplitudes is

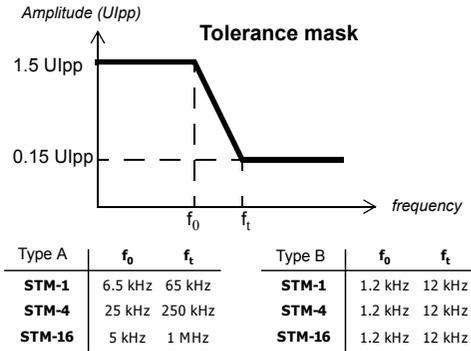


Figure 3.9 SDH optical regenerators, tolerance masks; ITU-T Rec. G.958.

expressed in dB. As with tolerance, the jitter introduced at the NE input to carry out the measurement is sinusoidal jitter.

One important aspect to consider is intrinsic jitter; that is, jitter generated inside the NE. To perform a correct transfer measurement, this intrinsic jitter must be subtracted from the output jitter; that is to say, the measurement must be calibrated. In transfer measurements, there is also the possibility to apply a filter to the NE output (as with output jitter). This depends on the measurement being performed (see Figure 3.10).

The function of jitter transfer $J(f)$ is:

$$J(f) = 20 \cdot \log \left| \frac{\text{OutputJitter} - \text{IntrinsicJitter}}{\text{InputJitter}} \right| (dB)$$

3.1.5.1 Jitter transfer in PDH and T-carrier

Recommendations G.742 and G.751 establish the jitter transfer requirements for plesiochronous multiplexers and demultiplexers. These requirements are set out in line with a set mask, in such a way that the performance specified for these NEs will be according to the tolerable jitter levels in an interface, as specified in ITU-T Rec. G.823 (see Figure 3.11). For T-carrier interfaces, the maximum tolerable jitter is defined by Telcordia GR-499, ANSI T1.403 (1.5 Mbps) and ANSI T1.404 (45 Mbps).

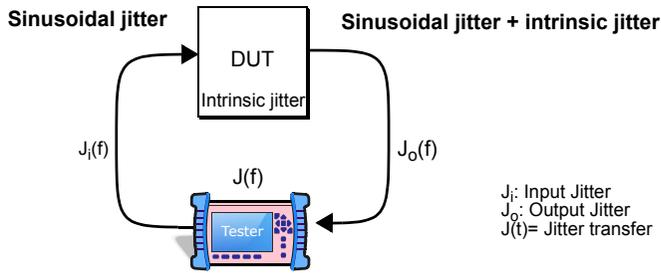


Figure 3.10 Set-up for measuring jitter transfer for each frequency.

3.1.5.2 Jitter transfer in SDH and SONET

To check jitter transfer between SDH/SONET synchronous interfaces, the NE under test must be synchronized with the input interface where jitter is generated, since the reference synchronization of the NE is actually what determines the timing of its STM-*n*/OC-*m* outputs. With this prior condition, it is established that the NE cannot amplify jitter above 2.3 % (0.2 dB) of the passband, which is determined by its clock recovery filter. This bandwidth typically reaches 1 Hz for NEs with G.813 category clocks (ETS 300 462-5); (see Figure 3.12). The equivalent Stratum 3 clocks are defined in ANSI T1.105.09 and Telcordia GR-1244.

Obviously, it makes sense to check the jitter transfer between the NE PDH tributary ports. In this case, the performance of the device must meet Recommendations G.742, G.751, and G.823.

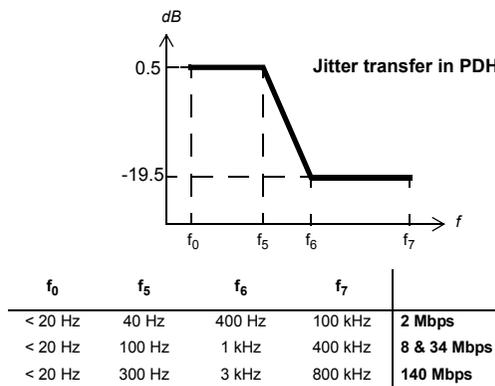


Figure 3.11 Jitter transfer mask for PDH. The numbering of the frequencies in the graph is not correlative, but no significant frequency is missing.

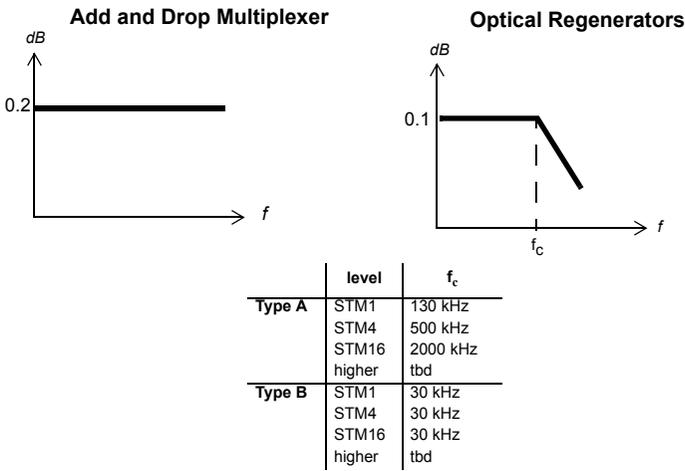


Figure 3.12 Jitter transfer masks for SDH on ADMs and optical regenerators.

3.1.6 Mapping Jitter and Combined Jitter

Jitter from phase quantization and desynchronization results in *mapping jitter* and *combined jitter*.

3.1.6.1 Mapping jitter

Mapping is the process through which PDH/T-carrier signals are introduced in SDH/SONET signals for transport. This takes place in multiplexers. The signal clock source is independent of the SDH clock source, so the PDH/T-carrier data is asynchronous from the SDH/SONET signals. In other words, the clocks of the tributary systems have no fixed relation with the multiplexer, or even between themselves. The tributary signals are asynchronous, that is, they allow deviations within a tolerance margin relative to their nominal clock value. This is where stuffing bits come in. They are used to resolve this asynchronicity, and in this way the PDH/T-carrier signal becomes part of the SDH/SONET payload which has a greater capacity. This excess capacity is filled with stuffing bits to obtain the constant rate specified for the container.

At the transmitting end, the bits of the tributary signals are continuously recorded in elastic memories, but are read discontinuously, because in order to proceed with their reading (and later transmission), these memories must first be filled; otherwise they would end up emptying completely. Reading is carried out at the highest possible rate, since the clock adaptation process performed by the multiplexer pro-

vides a transmission channel with a capacity higher than the sum total of the tributary rates plus the permitted tolerance (deviations relative to the nominal value). Since we want the reading clock to stop at times, but the output rate of the multiplexer aggregate signal must remain constant, stuffing bits are sent when there are no bits of information to be transmitted.

At the receiving end, these stuffing bits must be extracted to recover the tributary signals correctly. For this reason, these bits are not written in the elastic memories of the receiver. The frames contain indications that let them decide whether a bit is a stuffing bit or not. If the bit received is a stuffing bit, the writing clock is stopped. On reception, therefore, writing is discontinuous, whereas reading is continuous (since everything the memory contains forms part of the message).

On reception, the reading clock is derived from the writing clock by means of a *phase-locked loop* (PLL). Since the low pass filter of the PLL is not able to completely eliminate the discontinuities in the writing process, a residual phase modulation remains, and this is known as *mapping jitter* (also *stuffing jitter*).

3.1.6.2 Combined jitter

Mapping jitter is measured when there are no pointer adjustments in the aggregate signals. The pointer adjustment mechanism is one of the causes of jitter (pointer jitter), but this cannot be separated from mapping jitter, which is inherent in the generation of SDH/SONET signals. For this reason, pointer jitter cannot be measured separately from mapping jitter, and the fluctuation measured is known as combined jitter (see Figure 3.13).

Pointer jitter is the most important type of jitter found in SDH/SONET networks. It is the main cause of disturbance in hybrid PDH/SDH or T-carrier/SONET networks and, compared to mapping jitter, it is a component of much greater importance when it comes to measuring combined jitter. The cause of this type of phase fluctuation is the pointer adjustment mechanism, and it appears in those tributaries that, once disassembled (extracted from their virtual container), have undergone pointer changes along their path.

The pointer mechanism forms the basis of the SDH/SONET signal structure. For example, the essential difference between an SDH frame and a PDH frame is that in the former, the overhead information from the higher order signals is enough to determine the overhead position of the lower order signals. Pointers are values (divided into various bytes) that contain the position of the overheads. For example, for the mapping of 2-Mbps signals in SDH, two pointer levels are used. The higher level (AU-4 pointer) identifies where the VC-4 virtual containers start inside the STM-1 frame. The lower level (TU-12 pointer) identifies the start of a VC-12 virtual con-

tainer relative to the VC-4. In one STM-1 frame there will therefore be one AU-4 pointer and 63 TU-12 pointers.

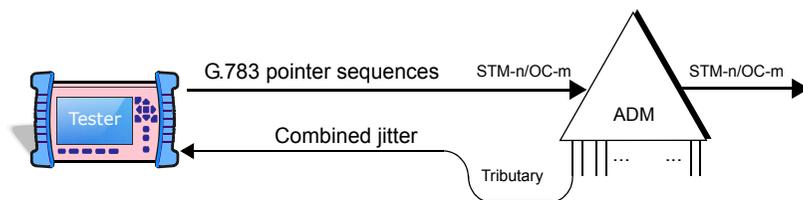


Figure 3.13 Combined jitter measurement, which includes pointer jitter.

When there are clear differences in the clock signals from two different networks or two different elements in the same network, it is necessary to compensate for these differences by *offsetting* the lower order signals into higher order (for example, VC-4 virtual containers in the STM-1 frame). This is achieved by increasing or decreasing the pointer value by one unit (depending on the appropriate adjustment at that time). The value of this offset depends on the pointer being adjusted. Returning to the case of mapping a 2-Mbps signal in SDH, an AU-4 pointer adjustment means an offset of 24 bits, whereas if it is a TU-12 pointer, the offset is of 8 bits. The AU-4 pointer adjustment contributes more to jitter, due to the fact that it appears more commonly than TU-12 pointer adjustment.

In any case, these offsets cause abrupt phase variations in lower order signals (tributaries). As with mapping jitter, the reading clock at the receiving end is derived from a PLL circuit. The lowpass filter in the control loop of the PLL tries to smooth out these phase shifts, but they nevertheless cause residual phase modulation to remain. This is pointer jitter, and it is the main contributor to combined jitter.

3.1.6.3 Measuring combined jitter

To check how effectively an NE compensates for the effects of pointer adjustments, some pointer adjustments are generated that have been specially designed to subject the element to stress, in such a way that the situations simulated might occur under normal conditions. A pointer adjustment is a change in its value, such as a unitary increment or decrement, for instance. Pointer sequences are defined in Recommendations ITU-T Rec. G.783, ANSI T1.105.03, and Telcordia GR-253. The measurement consists of checking the output jitter against this input stimulus. Combined jitter (which is largely pointer jitter) appears in the tributaries of a synchronous signal when these are extracted from the signal (see Figure 3.13).

3.1.7 Jitter in Leased Lines

Although tolerance to jitter is usually checked by means of sinusoidal stimuli, there are certain cases when this test is not performed this way; and such is the case with leased lines. In this type of system, it is necessary to have a method that characterizes and supplies more reliable results about the real jitter tolerance level than the results obtained by using frequency tones. The reason for this is that although these tones are useful for checking that the buffers are working correctly, they are not exact enough when it comes to reproducing the random characteristics of the jitter found in “real” systems.

For example, the ETSI has defined a series of broadband signals for checking jitter tolerance in leased lines. These take advantage of the random characteristics of the PRBS patterns, to modulate the phase of the data signal of the line (2 Mbps in the example), following the appropriate filtering. The jitter tolerance of the line is evaluated at the remote end, depending on the anomalies that appear, and the amount of output jitter.

3.2 DEALING WITH WANDER

To guarantee correct operation for SDH/SONET networks, the elements that make up these networks must be synchronized, that is, they must share a common reference clock. The common reference signal to which the clocks of the NEs themselves are synchronized, usually comes from high-quality clocks that act as a *primary reference clock* (PRC). Based on these clocks, the signal is distributed in a network of subsidiary clocks until it reaches the NEs. So, there is a network of clocks that synchronizes the SDH/SONET network.

Here, wander is a critical type of phase fluctuation, since it builds up in the synchronization chain. This slow phase fluctuation can often be observed on the boundary between two different SDH/SONET networks, each with its own PRC, and on the international boundaries where there are networks using different reference clocks. The causes of this wander are:

- Changes in the propagation delay of cables (temperature);
- Drifts in the PLLs of the clocks;
- Phase fluctuations due to reconfiguration of the synchronization chain, either by the operators themselves or by the automatic protection switching mechanism;
- Differences in frequency resulting from a loss of synchronization in a network node (limit of 4.6 ppm).

3.2.1 Synchronization of SDH/SONET Networks

A functional separation can be established between the SDH/SONET network and the network of clocks that synchronizes it (in some cases, even if this separation is not physical, as will be seen). Owing to the problem of wander in synchronization chains, the ITU, ETSI, ANSI, and Telcordia have produced some recommendations for limiting this phase fluctuation in all these clocks (PRC/PRS, SSU/BITS, and SEC), and guaranteeing that the SDH/SONET network operates correctly.

3.2.2 Measuring Relative and Absolute Wander

Given our understanding of wander as the difference of phase (or of time) between two clock signals, it is important to distinguish between relative and absolute wander measurement (see Figure 3.14).

The measurement of absolute wander at a given instant is equal to the phase difference that exists, at that moment, between the clock of a signal and UTC, as defined in ITU-T Rec. G.810, ETS 300 462-1, and ANSI T1.101. The effective quality provided by the synchronization network can be seen by carrying out this measurement which requires a high-quality clock source, derived directly from the UTC (such as that provided by a GPS receiver).

The measurement of relative wander at a given instant is the phase difference that exists, at that moment, between any two clocks in the network. It is very useful to carry out this measurement in two interfaces, when we want to check such aspects as wander generation in a synchronous element (checking the gap between input and output interfaces), the possible appearance of pointer adjustments between two STM-*n*/OC-*m* signals that converge in a single NE, and so on. In short, the difference between both types of measurement depends on the reference clock chosen: In the case of absolute measurement, the clock being measured is compared against the most stable reference that exists.

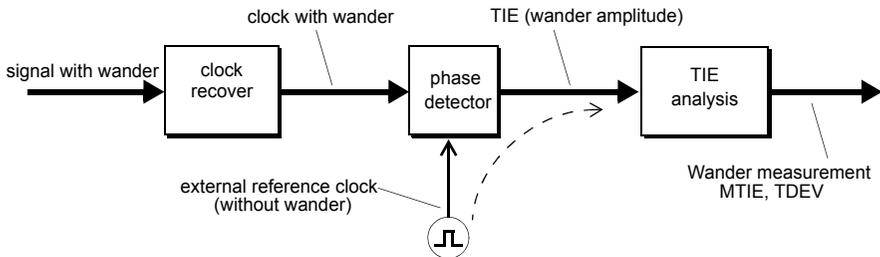


Figure 3.14 Wander measurement needs an external reference; otherwise it will take a lot of time to get a good recovered clock.

3.2.3 The Metrics of Wander: TIE, MTIE, and TDEV

Given that wander is a slow phase fluctuation (with spectral components below 10 Hz), wander measurements require long periods of time. It is also necessary to detect phase transients during these measurements, which calls for high temporal resolution, and, as a result, there is a considerable accumulation of data. With the aim of summarizing all this information, three parameters are defined below that are fundamental in measuring wander: TIE, MTIE, and TDEV.

3.2.3.1 TIE

The *time interval error* (TIE) is the slow phase fluctuation amplitude, which means that it indicates the phase variation of the clock to be measured, relative to the phase of an ideal reference clock during each instant of the measurement. Usually, TIE=0 is taken as a reference at the start of the measurement. The TIE can be and usually is expressed in absolute time (ns, μ s, ms), but it can also be expressed relative to the signal period (unitary intervals).

3.2.3.2 MTIE

The *maximum time interval error* (MTIE) is the maximum value of peak-to-peak TIE (TIE_{pp}) in a certain observation time, t . This means that in order to calculate the MTIE, a time window must be scrolled over the function TIE(t), recording the maximum peak-to-peak value of the TIE: TIE_{pp}. This can be repeated for different values of τ , thus obtaining a graph of MTIE (τ) (see Figure 3.15).

3.2.3.3 Application

The MTIE helps in obtaining realistic information on the buffer size of synchronous instruments. The buffers of digital instruments associated with clock recovery (PLL) allow frequency fluctuations to be absorbed, but their size must be limited, to avoid increasing latency. This size is calculated by using the MTIE (see Figure 3.15).

3.2.3.4 TDEV

Time deviation or TDEV is a measurement that characterizes the spectral content of a TIE(t) signal. This means that it measures the energy of wander frequency components. As is the case with MTIE, the TDEV is a function of the integration time τ . The functional diagram of a TDEV measurement circuit is shown in Figure 3.16.

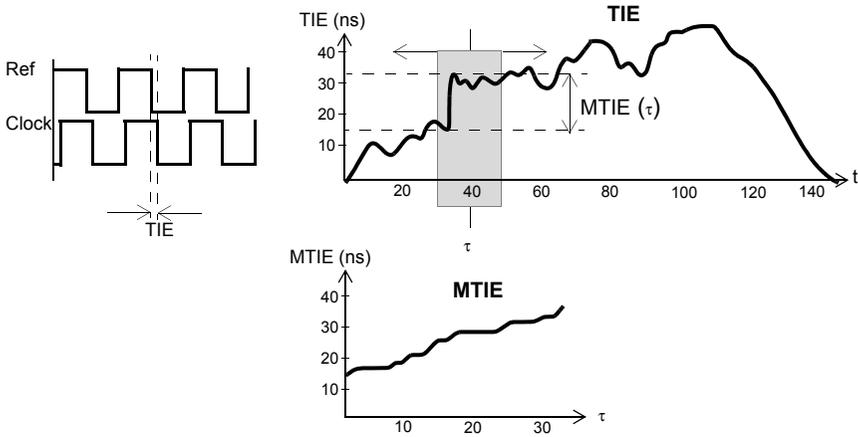


Figure 3.15 MTIE (τ): maximum peak-to-peak amplitude of the slow phase fluctuation or TIE in an observation window τ .

The first block, $H(f)$, is a filter with its passband $(0, 1/\tau)$ centered on the value $0.42/\tau$. The analysis is therefore limited to the passband mentioned before. The second block calculates the value of the root mean square (r.m.s.), which evaluates the energy of the components in the band being analyzed. By varying the value of τ , we can then analyze the different frequency bands that are of interest to us. The above considerations have ITU-T Rec. G.810 and ANSI T1.101 as their source.

For a correct calculation of the TDEV, it is recommended that the length of the measurement be 12τ , although 3τ is enough; that is, we must have samples of TIE in at least the time interval $0,3\tau$, with $t=0$ being the starting instant of the measurement. Given that the TDEV is an r.m.s. value, it is always positive, as a sum of square (see Figure 3.16).

3.2.3.5 Application

The TDEV lets us evaluate the short-term stability of the clock signal. We can characterize the transfer of wander in the NE used, in order to limit the buildup of this phase fluctuation (ETSI specifications on the transfer of wander between the ports of a synchronization source - clock - specify this transfer in terms of TDEV).

Furthermore, the TDEV converges for many types of phase noise, which makes it possible to identify the source and eventually correct the causes of degradation in transmission (see Table 3.1).

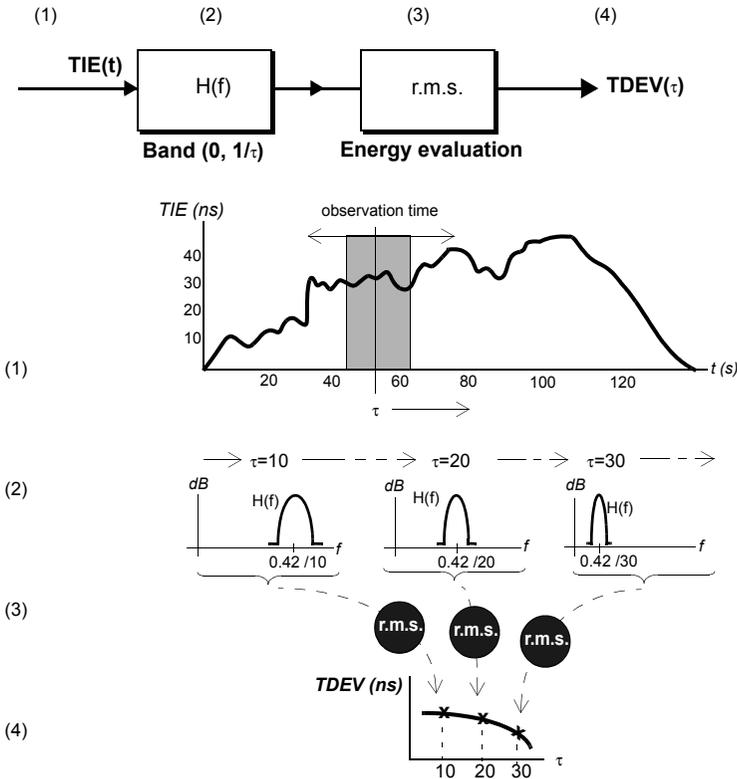


Figure 3.16 Calculation of the TDEV step by step. (1) for each window τ swept; (2) low pass filter; (3) measurement of r.m.s value; and (4) new TDEV point.

3.2.4 Measuring Output Wander

The aim of this measurement (as with jitter) is to quantify the amount of wander present in a network interface or a device. This quantification is usually made in terms of MTIE and TDEV (see Figure 3.17).

Synchronization signals are distributed through SDH/SONET sections (STM- n /OC- m) and PDH/T-carrier paths (2 or 1.5 Mbps). The ETSI Recommendation ETS 300 462-3 (PDH) and Telcordia GR-499 (T-carrier) establish masks showing the limits of MTIE and TDEV for these rates, where applicable. The synchronization interfaces at these rates in which output wander is measured are:

- PRC/PRS clock outputs;
- SSU/BITS clock outputs;
- SEC clock outputs;

Table 3.1
The TDEV converges for some types of noise, which makes it possible to investigate the causes of phase noise.

<i>Noise</i>	<i>Slope of the TDEV</i>
White noise phase modulation (WPM)	-1/2
Flashing phase modulation (FPM)	0
White noise frequency modulation (WFM)	1/2
Random walk frequency modulation (RWFM)	3/2

- PDH/T-carrier synchronism distribution outputs.

The masks refer directly to each type of interface, that is, the TDEV and the MTIE are represented relative to the output wander of a PRC, an SSU, an SEC or a PDH output.

3.2.5 Measuring Tolerance to Input Wander

Tolerance to wander is based on the same concept as tolerance to jitter: How much phase fluctuation can an NE withstand at its input without seeing any degradation in its operation? ITU-T Rec. G.823 and G.825, ANSI T1.105.03, and T1.102, and Telcordia GR-499 and GR-253 specify the tolerance to wander (and jitter) for the interfaces of NEs (see Figure 3.8). When we are dealing with tolerance to wander in synchronization input interfaces, ETS 300 462-4 and ETS 300 462-5 apply to SDH, while ANSI T1-101 and T1.105.09 apply to SONET, specifying this tolerance in terms of MTIE and TDEV by means of the corresponding masks for an SEC and an SSU/BITS. In any case, the tolerance specifications for SEC and SSU/BITS are in

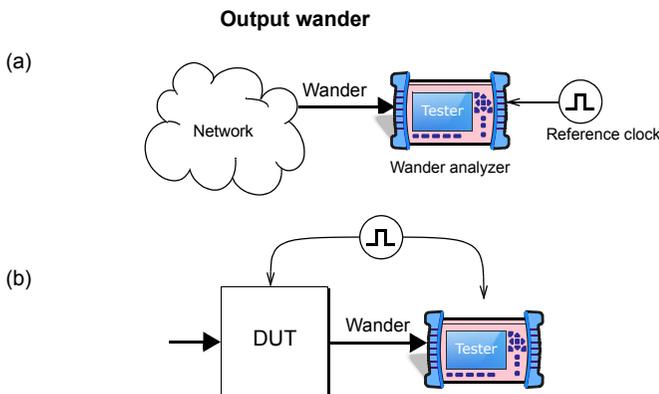


Figure 3.17 Measuring output wander: (a) in a network interface, the analyzer is synchronized with a clock free of wander; and (b) in the interface of a device; the device and the analyzer are synchronized using a common reference clock.

line with the maximum values for amplitude of phase fluctuation under ITU-T Rec. G.823 and G.825, and Telcordia GR-499 and GR-253.

Evaluating the tolerance of an SSU/BITS or an SEC consists of establishing the minimum values in terms of MTIE and TDEV in the input of the NE at which the SSU/BITS or SEC operates correctly, and comparing them with the corresponding masks (the values must be above or at least equal to those of the masks when operating correctly). By “operating correctly,” we understand that the following conditions are met:

- The clock remains within its margins of correct operation;
- No defects are shown;
- No switching of reference source takes place, or, if it does, this is without entering holdover mode.

These tolerance requirements are independent of the interface in which they are measured: 2 or 1.5 MHz, 2 or 1.5 Mbps or even STM-*n*/OC-*m* synchronous interfaces will do.

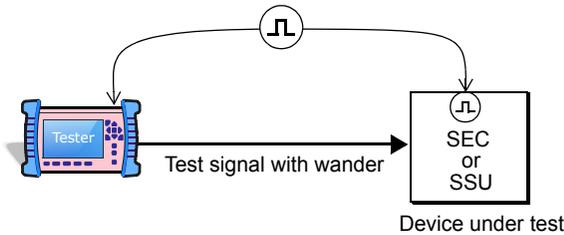


Figure 3.18 Measuring tolerance to input wander.

To measure tolerance to wander, the stimulus signal at the input (which may be 2 or 1.5 MHz, 2 or 1.5 Mbps or STM-*n*/OC-*m*) is usually subjected to a set wander modulation (see Figure 3.18). It may be sinusoidal although, for example, ETSI recommends the alternative of using broadband spectrum signals for this measurement, which should last at least 1,000 seconds.

For an SEC, tolerance is expressed in terms of TDEV in accordance with ETS 300 462-4 and ANSI T1.101, which define a mask. The phase modulation signal that is provided by the TDEV defined by this mask is a special (broadband) noise signal; the generation of which is also specified in its Annex C.

With regard to an SSU/BITS, tolerance to wander is expressed in terms of TDEV, and also of MTIE, and for special test signals that are adapted to these masks. Since the way of generating these special modulations is under study, a tolerance to wander mask is given as a valid alternative measurement when the phase modulation of the stimulus signal is sinusoidal.

The reference clock used in the measurements must always be of higher quality than the one in the DUT. For instance, if the tolerance of an SSU/BITS is being measured, the reference clock must be of PRC/PRS quality.

3.2.6 Measuring Wander Transfer

When the synchronization reference signal at the input of an NE contains wander, this is transferred to the STM- n /OC- m outgoing traffic signal, or to the output synchronization signal (see Figure 3.19). This transfer leads to an accumulation of wander in a chain of devices, and must therefore be limited. Recommendation ETS 300 462-4 and ANSI T1.101 define the limit of wander transfer, for an SSU, in terms of output TDEV.

In order to measure wander transfer in an SEC, Appendix B of the ETS 300 462-5 recommends five different methods, all of them valid and characterized by the different phase modulation in the stimulus signal at the input. The signal at the input to the DUT is usually a synchronization reference (see Table 3.2).

3.2.7 Response to Phase Transients

There are a number of different sources from which an SSU/BITS (be it integrated or SASE) or an SEC clock can take its synchronization input signal. This allows it to be programmed in such a way that if this synchronization signal should fail in some way, it will switch over to a secondary synchronization source, and reestablish its normal operating status. This switchover may be caused by:

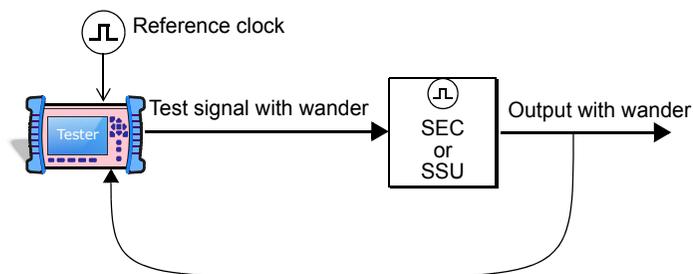


Figure 3.19 Measuring wander transfer.

Table 3.2
Phase modulations for the measurement of wander transfer in an SEC,
in line with ETS 300 462-5.

<i>Phase Modulation</i>	<i>Application</i>
Phase step	Devices that accept large phase transients or have a low level of internal noise.
Frequency step	This measurement method prevents the SEC from entering holdover or overflow occurring in the phase detector.
Sinusoidal	Found on devices with linear designs; its advantage is that the output can be selectively measured in terms of frequency.
Phase white noise (frequency domain)	Found on devices with nonlinear designs; also allows SEC to be characterized in frequency.
Phase white noise (time domain)	Response of SEC can be characterized in the time domain using a set measurement plan.

- Interruption of the reference signal;
- Phase skipping in the synchronization input due to reconfiguration in the synchronization chain;
- Frequency deviation in the reference signal; or
- An AIS defect in the 2 or 1.5-Mbps reference signal (when used).

During switchover, a transient period occurs within which the phase of the output clock of the SSU or the SEC undergoes shifts. In short, a phase error or excursion occurs in the synchronization output signal relative to the input signal at the instant when the reference is lost. Since the wander in the output of a synchronization chain is limited, it is necessary to limit this phase error as well (see Figure 3.20). For example, in SDH there is a phase error limitation curve (ETS 300 462) (see Figure 3.21). In this case, switching to a secondary reference source is considered to be *short term*, which means that it takes place *quickly*.

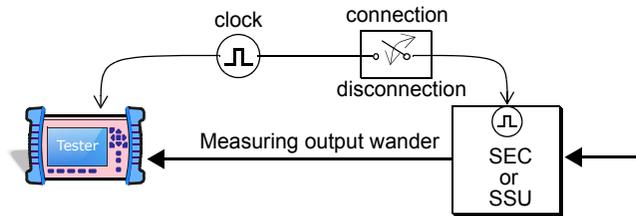


Figure 3.20 Transient due to reference switching.

The curve limits the maximum phase error (E_{max}) and the maximum duration for the transient (T_{max}). For instance, in the case of an SEC, $E_{max} = 1$ ms and $T_{max} = 15$ s for the configuration of measuring the phase error (TIE) (see Figure 3.22).

In the case of an SEC, then, the response to the transient is measured by evaluating the TIE from which the reference is disconnected until it connects again 15 s later, and comparing this with the corresponding curve in ETS 300 462 5.

3.2.8 Operating in Holdover Mode

When the reference source is lost and the switching transient goes beyond a certain time (15 seconds for an SEC), reference switching is said to be long term. In this case, the clock enters holdover mode. The restrictions with regard to the phase error are different from those presented in the section above.

3.2.8.1 Holdover

In holdover mode, the SSU/BITS or the SEC use statistics from the source with which they have been synchronized (frequency, frequency drift, etc.) to provide a timing that is as similar as possible to the one they had been supplying. As this is extended, the phase error on output will increase, owing to such factors as variations in temperature, aging of the unit, and so on.

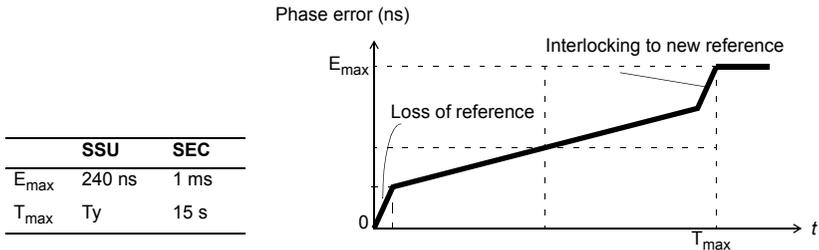


Figure 3.21 Limit-curve of transient due to short-term reference switching; ETS 300 462-4 for SSU and ETS 300 462-5 for SEC.

3.2.8.2 Measuring phase error in holdover

The measurement configuration is the same as for short-term switching measurement. In this case, it is necessary to compare the measurement results with the corresponding phase error restrictions for this mode. For example, as with short-term

switching, Recommendations ETS 300 462-4 (for SSU) and ETS 300 462-5 (for SEC) give limit-curves, which can be expressed by the following function:

$$DT(S) = \{(a_1 + a_2) \cdot S + 0.5 \cdot b \cdot S^2 + c\};$$

where: S: holdover time ($S > 15s$ or T_y);

DT(S): phase error

a_1 : maximum value of initial frequency offset;

a_2 : offset due to variations in temperature, if these occur;

b: frequency drift due to aging of the unit;

c: phase skipping that occurs when entering holdover.

The values for an SSU and an SEC are different (see Table 3.3).

Table 3.3
Parameters of phase error due to long-term reference switching (holdover) for an SSU and an SEC.

	SSU	SEC
a_1	0.5 ns/s	50 ns/s
a_2	2.0 ns/s	2,000 ns/s
b	2.3×10^{-6} ns/s ²	1.16×10^{-4} ns/s ²
c	60 ns	120 ns

The corresponding phase error curves are shown. Here, it is assumed that there is no offset due to temperature variation (see Figure 3.22).

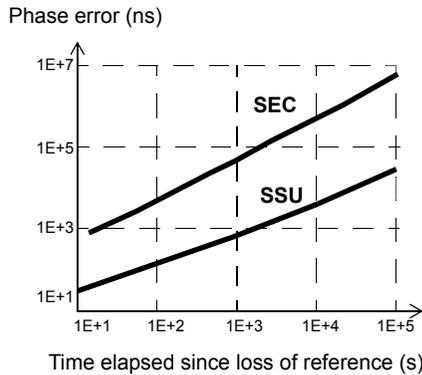


Figure 3.22 Limit-curve of transient due to reference switching in holdover; ETS 300462-4 for SSU and ETS 300 462-5 for SEC.

3.3 TESTS ON ADMs AND CROSS-CONNECTS

Acceptance tests must be carried out on NEs once they have been purchased, to check that they are operating correctly.

3.3.1 Measuring Jitter

In this example of acceptance, mapping jitter and combined jitter are measured in an ADM. Basically, these are measurements of jitter amplitude in the multiplexer tributary ports (output jitter).

3.3.1.1 Measuring mapping jitter in an ADM

Measuring mapping jitter consists of generating an aggregate signal with a PDH or T-carrier test payload that has a frequency offset with respect to its nominal value. This payload is unmapped in the ADM, and analyzed to quantify the jitter it presents. The conditions under which the measurement is made are as follows (see Figure 3.23):

1. Three frequency offset values are generated for the test signal: 0 ppm, +50 ppm, and -50 ppm.
2. For each offset generated, two jitter amplitude values are obtained: one corresponding to a band of frequencies from 20 Hz to 100 kHz, and another corresponding to a band of frequencies from 18 kHz to 100 kHz.
3. For both frequency bands, the measurement interval is 60 seconds.
4. The measurement is repeated regularly for a tributary from each tributary card in the multiplexer, and for both aggregate sides, although this depends on the stipulations of the acceptance protocol for each operator.

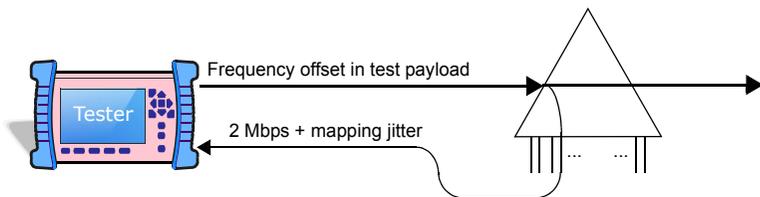


Figure 3.23 Set-up for measuring mapping jitter.

3.3.1.2 Measuring combined jitter in an ADM

Measuring combined jitter (pointers plus mapping) consists of generating TU pointer adjustment sequences over the TU pointer associated with the virtual con-

tainer of the PDH/T-carrier test signal in the aggregate signal. The response to these adjustment sequences (defined by ITU-T Rec. G.783, ANSI T1.105.03, and Telcordia GR-253) is the jitter measured in the associated tributary signal.

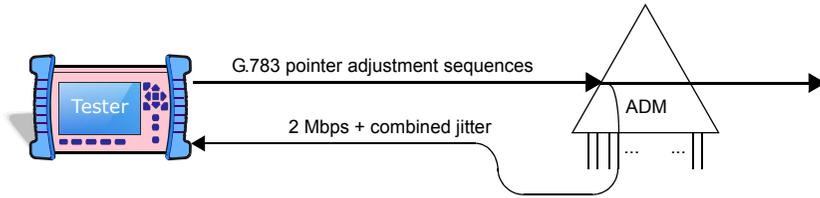


Figure 3.24 Set-up for measuring combined jitter.

The conditions under which the measurement is carried out are:

1. Two types of adjustment sequences are generated:
 - Isolated adjustments of alternate TUs¹ or VTs;
 - Single TU adjustments with double TU or VT adjustment².
2. For each offset generated, two jitter amplitude values are obtained: one corresponding to a band of frequencies from 20 Hz to 100 kHz, and another corresponding to a band of frequencies from 18 kHz to 100 kHz.
3. For both frequency bands, the measurement interval is 60 seconds.
4. As with mapping jitter, the measurement is repeated regularly for a tributary from each tributary card in the multiplexer, and for both aggregate sides, although this depends on the stipulations of the acceptance protocol for each operator.

The measurement set-up is similar to the one used for measuring mapping jitter (see Figure 3.24).

-
1. Isolated adjustments of alternate TUs: This sequence provokes a single pointer adjustment every 10 seconds with alternate polarity. A positive adjustment increases the pointer value by one unit, and a negative adjustment decreases it by the same amount; in both cases the phase is offset by 8 bits (8 UI) (see Figure 3.25).
 2. TU with double TU adjustment: This sequence provokes cycles of four pointer adjustments with 0.75 seconds between them, except for the third, which is a double adjustment with a separation of 2 ms. All the adjustments have the same polarity (see Figure 3.25).

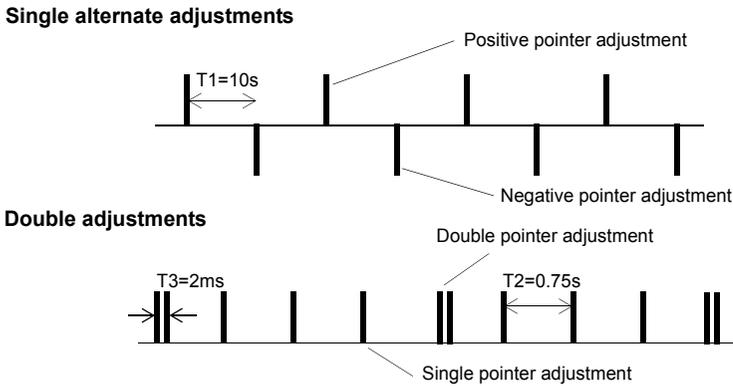


Figure 3.25 ITU-T Rec. G.783 sequences. Single alternate adjustments and regular adjustments with double adjustments.

3.3.2 Synchronization Tests

Synchronization can be distributed to the SDH/SONET network elements in two ways, either from the synchronization network (separate from the SDH transport network), or by using the transport network itself. When a loss of external synchronization occurs, the SEC of an NE can act independently, either in holdover or in free-running mode. In the first case, the synchronization signal is reconstructed based on the data from the synchronization source previously connected. In the second case, the NE obtains the synchronization signal from its own internal clock.

In free-running mode, the NE clock must maintain a certain level of exactitude, as stated in ITU-T, ANSI, and Telcordia recommendations. This test checks whether an NE is operating correctly in free-running mode, and when it receives its synchronism reference signals through the transport network.

3.3.2.1 Free-running test

This situation comes about, as stated above, when the NE does not have an external synchronization signal, and has to obtain its signal from its internal clock. ITU-T Rec. G.813, ANSI T1.105.09, and Telcordia GR-1244 determine that the exactitude of output frequency of an SEC with respect to PRC must not be greater than 4.6 ppm.

The free-running test verifies this requirement, as well as checking that tributaries have been correctly extracted in the corresponding ports of the element under test. To carry out this test, the tributary input must be disconnected. This will provoke the switchover to free-running mode, and the element under test (ADM in this

example) will generate an AIS signal that will be received by the analyzer from the tributary output at the free-running frequency within the tolerance margin, $f_{0nom}+4.6 ppm, f_{0nom}-4.6 ppm$. One possible procedure for carrying out this test is the following (see Figure 3.26):

1. Offset the frequency of the tributary signal generated f_1 to a value within the tolerance margin, $f_{1nom}+50 ppm, f_{1nom}-50 ppm$, and check that the frequency of the tributary signal recovered on extraction coincides with the value within the margin ($2,048,000\pm 102 Hz$).
2. Check that the frequency of the signal in the ADM synchronization output does not vary when f_1 varies, and that it is within the tolerance margin, $f_{0nom}+4.6 ppm, f_{0nom}-4.6 ppm$, that is, $2,048,000 \pm 9 Hz$, in accordance with the recommendations.
3. Disconnect the tributary signal generated at the input port. As a consequence of this loss of signal, the ADM will have to generate an AIS that the 2-Mbps analyzer will receive at the tributary output. The frequency value of this signal must remain within the margin, $f_{2nom}+4.6 ppm, f_{2nom}-4.6 ppm$, that is, $2,048,000 \pm 9 Hz$.

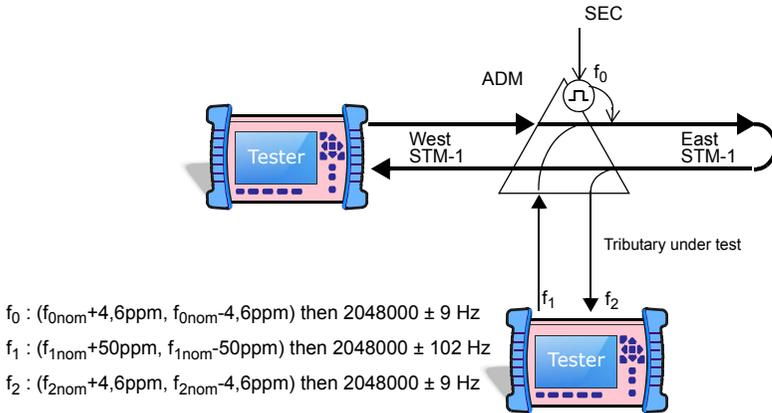


Figure 3.26 Free-running test.

3.3.2.2 Synchronization reference switching (I)

This test checks the switching from the primary reference source (in this example, the SDH generator) to a secondary reference, which in this case will be the internal clock of the NE (free running).

The ADM takes its synchronization from the West aggregate signal (STM-1 W) that the generator of the tester provides as a primary reference, disabling its synchronization input for a secondary reference if the first one fails. The internal clock of the ADM will then take on the role of secondary reference. Likewise, the primary synchronization output will be enabled to follow the primary synchronization input.

The test is performed by disconnecting the West aggregate input. The ADM then switches over to free-running mode, that is, secondary synchronization. The tributary analyzer must not register anomalies or defects, and the tributary frequency must remain constant.

As in the previous case, the capacity of the testers is used to measure the frequency of the tributary signal analyzed, checking that it remains unchanged during the switchover from one reference source to another.

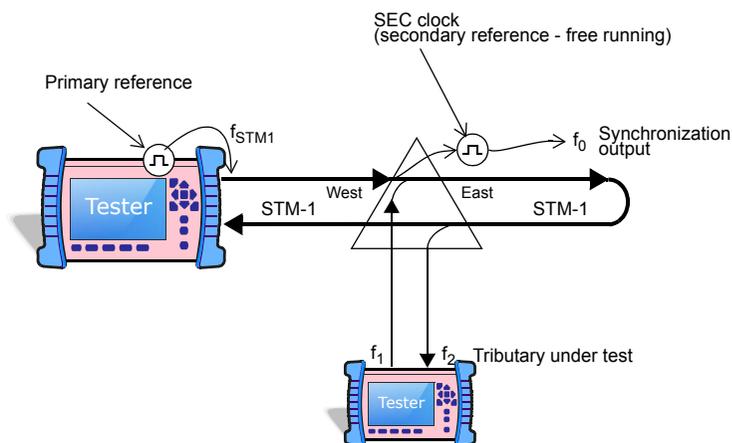


Figure 3.27 Synchronization reference switching.

One way of performing the test could be the following (see Figure 3.27):

1. Offset the frequency of the tributary signal generated, f_1 , to a value within the tolerance margin, $f_{1nom} + 50 \text{ ppm}$, $f_{1nom} - 50 \text{ ppm}$, and check that the frequency of the tributary signal recovered on extraction coincides with the value within the margin, $2,048,000 \pm 102 \text{ Hz}$. This checks that the tributary has been recovered correctly. For the rest of the test, program the frequency:

$$f_1 = f_{1nom} + 25 \text{ ppm}.$$

2. Vary the frequency f_{STM1} a few ppm and see that the frequency of the ADM synchronization output, f_0 , varies by the same amount. You must also check

that the frequency f_2 is not affected by these variations.

3. Program the frequency of the West aggregate to the value of $f_{STM1nom} + 5ppm$. The frequency meter applied to the synchronization output should measure approximately $2,048,010$ Hz, that is, $2,048,000 + 5 ppm$, the synchronization output moves the same amount of ppm as the synchronization reference.¹
4. Disconnect the West aggregate input. This way, the ADM loses its primary synchronization source and, because it does not have a secondary synchronization source programmed, it enters into free-running mode. In this mode:
 - The 2 Mbps analyzer must not register anomalies or defects;
 - The f_2 frequency of the tributary analyzed must not vary only because it has switched from one synchronization reference to another;
 - f_0 takes the value of free running frequency;
 - The corresponding defects appear in the user interface (UI) of the ADM control computer.
5. Connect the aggregate input to the SDH generator again. The following should be observed:
 - The defect indications disappear from the UI of the control computer;
 - The synchronization reference switching from the internal clock of the ADM to the aggregate signal does not affect the value of the f_2 frequency;
 - No anomalies or defects are registered in the 2-Mbps signal analyzed;
 - The ADM synchronization output signal takes on the frequency value of $2,048,010$ Hz again, and follows the frequency variations of the West aggregate signal.

3.3.2.3 Synchronization reference switching (II)

This test checks the switching from the primary reference source to a secondary reference; both of these being aggregate signals (see Figure 3.28). In this example, the NE takes its synchronization from the East aggregate signal (STM-1 E) as its primary reference, and from the West aggregate (STM-1 W) as secondary reference, should the first fail. The internal clock of the element will therefore take on the role of a tertiary reference, coming into action (free running) if the other two fail.

Likewise, the primary synchronization output will be enabled to follow the primary synchronization input, and the secondary synchronization output will follow

1. The difference between this value and the frequency value obtained for free running in the previous test ($2,048,000 \pm 9$ Hz). This makes it easy to distinguish between the West aggregate acting as a synchronization reference and operation in free-running mode.

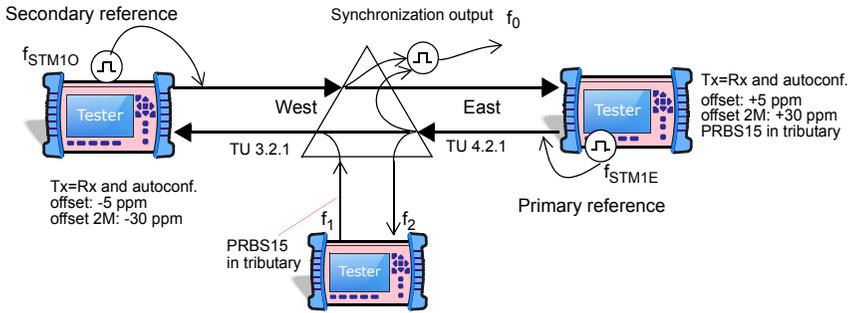


Figure 3.28 Synchronization reference switching (II).

the secondary synchronization input. To carry out the test, it will be checked that the synchronization output follows the frequency variations of the primary source (East).

The primary source will also be disconnected to provoke the switchover to the West reference, checking that the synchronization output now follows the variations of this aggregate. Finally, the West aggregate will be disconnected so that the ADM enters into free-running mode, checking that an AIS is received in the tributary analyzed at the free-running frequency (which has been previously measured).

As in the above measurements, the capacity is used to measure the frequency over the signals analyzed, checking their expected values at each stage of the measurement, in line with the operative reference sources.

Procedure for carrying out the reference switching

1. The primary synchronization reference is supplied by the East side tester. Check that the primary synchronization output (f_0) of the ADM follows the frequency variations of the East aggregate. Next, introduce an offset of +5 ppm: $f_{STM1E} = f_{STM1nom} + 5 \text{ ppm}$ ($155,520,000 \text{ Hz} + 778 \text{ Hz} = 1,555,520,778 \text{ Hz}$). Check also that the frequency f_2 varies with the frequency of the TU 2.4.1 tributary by changing the offset of this tributary. Set this offset at +30 ppm: $f_2 = f_{2nom} + 30 \text{ ppm}$ ($2,048,000 \text{ Hz} + 61 \text{ Hz} = 2,048,061 \text{ Hz}$). This part of the test checks that the synchronization is correctly extracted from the East aggregate.
2. When the East aggregate input is disconnected, the following must be observed:
 - No anomalies have occurred in the TU 3.2.1 received in the West side;
 - The 2-Mbps analyzer receives an AIS. Note its frequency value (f_2);

- The primary synchronization output frequency (f_0) has changed to the value associated with the secondary reference (West signal with offset of -5 ppm), that is, 2,047,990 Hz; and
- The control computer displays the corresponding synchronization defects.

This stage of the test checks that the switching between primary and secondary synchronization sources is correct.

3. The analyzer section of the 2-Mbps device should now be connected to the output of tributary port. Check that:
 - The synchronization output frequency of the ADM (f_0) follows the frequency offsets of the West aggregate ($f_{STM10} = f_{STM1nom} + offset$), and then set the value at $f_{STM10} = f_{STM1nom} - 5 ppm$.
 - The frequency of the signal from the tributary (f_2) follows the variations introduced from the West side SDH generator in the TU 3.2.1. Set this offset at -30 ppm:
 $f_2 = f_{2nom} - 30 ppm (2,048,000 Hz - 61 Hz = 2,047,939 Hz)$.
4. When the West aggregate input is disconnected, the following must be observed:
 - No anomalies are detected in TU 3.2.1;
 - The 2 Mbps device receives an AIS signal. Check that the value of f_2 coincides with the value noted in step 2;
 - f_0 changes to the free-running frequency value measured in step 2 of the test on the ADM in free-running mode;
 - The control computer displays the corresponding synchronization defects.
5. Connect the West aggregate input again and check that:
 - The ADM switches its reference to the STM-1 West signal (secondary). To do so, measure $f_2 = f_{2nom} - 30 ppm (2,048,000 Hz - 61 Hz = 2,047,939 Hz)$ and $f_0 = f_{0nom} - 5 ppm (2,047,990 Hz)$ to check that this switching has taken place correctly;
 - The control computer displays the corresponding synchronization defects.
6. Connect the East aggregate input again and connect the output of tributary port to the 2 Mbps analyzer. Check that:
 - The ADM switches to its primary reference by measuring $f_2 = f_{2nom} + 30 ppm (2,048,000 Hz + 61 Hz = 2,048,061 Hz)$ and $f_0 = f_{0nom} + 5 ppm (2,048,010 Hz)$;
 - The control computer no longer shows any synchronization defects.

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Index

A

Acceptance tests 107
Add and drop multiplexer (ADM) 7, 75
Administrative unit (AU) 11
Administrative unit group (AUG) 15
AIS 46
 AU-AIS 49
 MS-AIS 48
 PDH-AIS 49
 TU-AIS 49
Alarm 41
Alarms
 SDH 41
Aligning 11, 19
Anomaly 38
APS 51

B

BER 45
 penalty 89
B-ISDN 1
Bit error 70, 83
Bit interleaved parity (BIP) 44
Bit stuffing, *see* Stuffing
Bose-Chaudhuri-Hocquengheim (BCH) 45
Broadband-ISDN, *see* B-ISDN
Building integrated timing supply (BITS) 65, 75

C

Channel
 embedded 58
Clock
 master 61, 63, 75
 performance of 63, 73
 PLL 96, 98
 PRC 74, 75, 96

PRS 74, 75
recovery 71
reference 96
sampling 70, 83
SEC 74, 75, 101, 102, 109
signal 70, 83
slave 62
transfer
 SONET/SDH 66
 T-carrier/PDH 65

Combined jitter, *see* Jitter
Common management information protocol (CMIP) 57
Concatenation
 contiguous 38
 definition 37
 virtual 18, 37, 38, 50
Cross-connect 107

D

Damage 41
Defect 41
 definition 46
Demultiplexer, *see* NE
Desynchronization 93
Digital cross-connect (DXC) 7, 75
Digital video broadcasting (DVB) 18

E

East aggregate 112, 113, 114
 see also West and West-East aggregate
Enhanced remote defect indication (E-RDI) 49
Error
 monitoring
 definition 44
 onset of 89

Ethernet 18
 GbE 30
 LAPS 18
 SDH 18

Events 41
 monitoring of 41

F

Failure 41
 FEC 45
 Frame
 E1 77
 PPP 18
 STM 20, 21, 23, 35, 36
 STS 20
 T1 77

Frequency offset 68, 107

G

G.7041 18
 G.7042 18
 G.707 11, 18
 G.742 92
 G.751 92
 G.783 95, 108
 G.810 72, 97, 99
 G.813 92, 109
 G.823 85, 88, 89, 91, 92, 101, 102
 G.825 86, 88, 89, 102
 G.958 88, 89
 Generic framing procedure (GFP) 18
 Global positioning system (GPS) 67

H

Higher-order path (HP) 9
 Holdover mode 67, 80, 105
 definition 63
 operating in 105
 phase error 105

I

Indication 41
 Interface
 input 88
 output 88

PDH
 jitter 85
 Q 58
 T-Carrier 91
 X 58

Internode 65
 Interval, see Unitary interval (UI)
 Intranode 65

J

J-bit 26
 Jitter 27, 70, 83, 84
 ADM 107
 amplitude 89
 masks 88
 combined 93
 definition 94
 measurement 95
 definition 71
 demapping 71
 digital signal 84
 intrinsic 91
 leased lines 96
 mapping 71, 93, 107
 definition 94
 measurement filters 85
 metrics 84
 output 87, 91
 pointer 71, 94, 95
 regenerators 71
 sampling errors 71
 SDH 71
 see also Phase
 sinusoidal 89
 SONET 71
 stuffing jitter
 definition 94
 tolerance 88, 89
 definition 88
 masks 89
 transfer 90
 PDH/T-Carrier 91
 SDH/SONET 92
 Justification
 phase 71

L

- Layer
 - physical 10
 - seven-layer model 57
- Line section 10
- Line terminal multiplexer, *see* LTMUX
- Link capacity adjustment scheme (LCAS) 6, 18
- Local area network (LAN) 18
- Lower-order path (LP) 9
- Lower-order path, *see* LP
- LTMUX 7

M

- M.3000 57
- Management entity 57
- Management information base (MIB) 58
- Mapping 11, 19, 21
 - asynchronous 20, 22, 23
 - definition 93
 - see also* Jitter
 - see also* Multiplexer, Multiplexing
 - see also* Signal
 - synchronous 23
- Master clock, *see* Clock
- Maximum time interval error (MTIE), *see* Wander
- Measurement filters
 - highband 86
 - wideband 85
- Measurement interval 86
- Measurements
 - combined jitter 95
 - jitter and wander 85
 - jitter in output interfaces 87
 - jitter tolerance 88
 - jitter transfer 90
 - mapping jitter 107
 - output wander 100
 - relative and absolute wander 97
 - wander transfer 103
- Modulation
 - see* Phase
- Monitoring
 - errors 44
 - events 41
 - performance 44

- MSSPRING 54
- MTIE, *see* Wander
- Multiplex section dedicated protection ring (MSDPRING) 53
- Multiplex section linear protection (MSLP) 53
- Multiplex section overhead, *see* SOH
- Multiplex section protection (MSP) 53
- Multiplexer
 - mapping 93
 - See also* ADM
- Multiplexer section (MS) 10
- Multiplexer, *see* NE
- Multiplexing 11, 19, 20, 21, 23, 71

N

- NE 6, 44, 74, 92, 101, 112
 - acceptance tests 107
 - ADM
 - Measuring jitter 107
 - Synchronization reference switching 110
 - Synchronization tests 109
 - tests on 107
 - demultiplexer 88
 - free running mode 109
 - holdover 63
 - input and output interfaces 88
 - jitter 88, 90
 - multiplexer 88
 - pointer adjustments 95
 - regenerator 6, 88
 - regenerator section 7
 - STE 6
- Network
 - asynchronous 63
 - plesiochronous 63
 - security 49
 - synchronization 64, 75, 79
 - definition 61
 - synchronous 3
 - See also* Topology
- New data flag (NDF) 27, 29
- Node 8, 26, 73
 - interconnection 65
 - internode 65
 - intranode 65

O

O.150 88
 O.171 89
 O.181 88
 OAM functions 57
 Open systems interconnection (OSI) 57
 Operation support system (OSS) 57
 Operation, administration and management (OAM), *see* OAM functions
 Output jitter, *see* Jitter
 Overhead addition 11
 Overhead block 12

P

Packet
 over SDH/SONET (PoS) 18
 Path
 layer, definition 9
 Path overhead, *see* POH
 Path terminal equipment (PTE), *see* PTE
 Payload
 block 12
 synchronization 26
 PDH
 clock transfer 65
 jitter transfer 91
 limitations 1
 synchronization 73
 transport of tributaries 19
 Performance
 clock 63
 monitoring of 44
 Phase
 error 106
 fluctuation 70, 83, 84, 85, 94, 96
 slow 99
 justification 71
 modulations 104
 quantization 86, 93
 see PLL
 transient 98, 103
 See also PLL
 Phase-locked loop, *see* PLL
 Plesiochronous
 definition 3
 PLL 71, 72, 78, 94, 95, 96, 98
 POH 13, 30, 31, 32

4 bytes 33
 9 bytes 33
 higher-order 33
 lower-order 33
 Point to point protocol (PPP) 18
 Pointer 13, 26, 37
 adjustment 26, 83, 88, 94, 95
 decrement 28
 definition 94
 format 27
 generation 27
 increment 28
 procedures 27
 see Jitter
 sequence 95
 PRC, *see* Clock
 Primary reference clock (PRC), *see* Clock
 Primary reference source (PRS), *see* Clock
 75
 Protection
 1+1 51
 1÷n 51
 active and passive 51
 automatic protection switching 51
 bridge/switch signals 53
 dedicated and shared 51
 dual-ended or single-ended 52
 line 53
 multiplex section 53
 revertive or nonrevertive 52
 ring-switching or span-switching 52
 subnetwork 55
 trail or subnetwork 52
 types of 50, 51
 unidirectional or bidirectional 51
 virtual container path 55
 working or protection resources 51
 See also Test 50

Q

Quantification 100
 Quantization, *see* Phase

R

Reference clock 96
 Regenerator section (RS) 7, 10

Regenerator section overhead, *see* SOH

Regenerator, *see* NE

Regenerator, *see* NE

Resilience

 protection 50

 restoration 50

Resilient packet ring (RPR) 18

S

Sampling 70, 83

 errors 71, 73

SDH 1, 18, 26, 27, 30, 35, 39

 clock transfer 66

 defects 49

 Ethernet 18

 events 38, 41, 46

 analysis 47

 layers 8

 malfunction 38

 multiplexing map 15

 performance monitoring 44

see Jitter

 synchronization 61, 75, 97

 timing 26

SDH/SONET

 clock transfer 66

 pointers, use of 71

 protection 50

 restoration 50

 security 49

 synchronization 74

 models 75, 76

SEC, *see* Clock

Section overhead, *see* SOH

Section terminating equipment, *see* NE

Section, *see* Regenerator section (RS)

Seven-layer model 57

Signal

 aggregate 94

 analog 65

 broadband 96

 clock signal 65, 70

 digital 65

see Jitter

 E1 65, 66

 higher order 95

 lower order 95

 offset 95

see also Clock

see also East aggregate, West aggregate

see Phase

 significant instant 70, 83

 square wave 83

 synchronization 26, 65, 68

 T1 65, 66

 tributary 71, 94

Signaling

 APS 30

Simple network management protocol (SNMP) 57

Slave, *see* Clock

Slip 61, 78, 83

SOH 33

 LOH 35

 MSOH 20, 33, 35, 46

 RSOH 10, 20, 33, 46

SONET 1, 5, 39

 comparison of SDH and 5

 events 41

 formats and procedures 11

 frame structure 12

 hierarchy 35

 jitter 71

 layers 8

 line section 10

 malfunction 38

 multiplexing map 15

 path layers 9

 pointers 27

 section 10

see Jitter

 synchronization 61, 97

 virtual tributaries 13

See also SDH 38

STM 12, 21, 23, 35, 36, 112

See also Frame

STS 20, 27, 33, 35, 36, 43, 58

STS-1 12

Stuffing 11, 63, 73, 93

 bits 94

 jitter, definition 94

Subnetwork 8, 55

Subnetwork connection protection (SNC-P)

55

- Switching
 - digital 77
 - Synchronization 112
 - bad 61, 71
 - definition 61
 - desynchronization 93
 - digital 77
 - hierarchical 61
 - models 75, 76
 - mutual 63
 - network 64
 - elements of 61
 - SDH and SONET 64, 66, 97
 - topologies of 63
 - payload 26
 - PDH 73
 - SDH/SONET 74, 75
 - signal 65, 68
 - T-carrier 73
 - tests of 109, 110
 - Synchronization status messages (SSM) 67
 - Synchronization supply unit (SSU) 65, 74, 75, 79, 101, 103
 - Synchronous digital hierarchy (SDH), *see* SDH
 - Synchronous equipment clock (SEC), *see* Clock
 - Synchronous optical network, *see* SONET
 - Synchronous transmission module (STM), *see* STM
 - Synchronous transport signal (STS), *see* STS
- T**
- Tandem connection monitoring (TCM) 45
 - T-Carrier 85, 91, 101
 - jitter transfer 91
 - mapping 93
 - T-carrier 74
 - clock transfer 65
 - synchronization 73
 - transport of tributaries 19
 - TDM 71
 - Tests
 - free-running 109
 - synchronization 109
 - Threshold 89
 - TIE 99, 105
 - definition 98
 - see* MTIE
 - wander metrics 98
 - Time deviation (TDEV) 102
 - application 99
 - calculation 100
 - definition 98
 - wander 98
 - Time interval error (TIE), *see* Wander
 - Timing
 - external 75
 - internal 76
 - line 75
 - through 75
 - transparency 66
 - Timing loop 77
 - Topology 8
 - distributed 64
 - hub/star 8
 - meshed 7, 64
 - mixed 7
 - ring 7, 64
 - tree 63
 - Transmission
 - security 49
 - Tributary signal, *see* Signal
 - Tributary unit (TU) 11
 - Tributary unit groups (TUG)
- U**
- Unidirectional path switched ring (UPSR) 56
 - Unitary interval (UI) 87
 - definition 84, 85
- V**
- Virtual container 12, 20, 21
 - higher-order 21
 - lower-order 21
 - POH 32
 - protection 55
 - Virtual tributary path (VT Path) 9
- W**
- Wander 27, 70, 83, 84, 96, 97
 - absolute 97
 - clock performance 73

- definition 72
- input tolerance 101
- MTIE 98
 - application 98
 - definition 98
- phase fluctuation 96
- phase modulations 104
- phase transient 98
- relative 97
- see also Phase
- TDEV 98
 - definition 98
- temperature changes 73
- TIE 98
- transfer
 - measurement of 103
- West aggregate 111, 112, 114

X

X.86 18

